64000

HP64000 Logic Development System

Model 64500S Positive PROM Programmer

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

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HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

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ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

SERVICE MANUAL

MODEL 64500S

POSITIVE PROM PROGRAMMER

REPAIR NUMBERS

This manual applies directly to Models with Repair Numbers prefixed 2239A. It also applies to Models that have Repair Numbers prefixed 1924A that have the 64501-66502 board installed. Section VII is the Manual Backdating section for Models with Repair Numbers prefixed 1924A that have the 64501-66501 board installed.

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Logic Systems Division
Colorado Springs, Colorado, U.S.A.

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Manual Part Number: 64500-90910
Microfiche Part Number: 64500-90810

Printed: October 1982

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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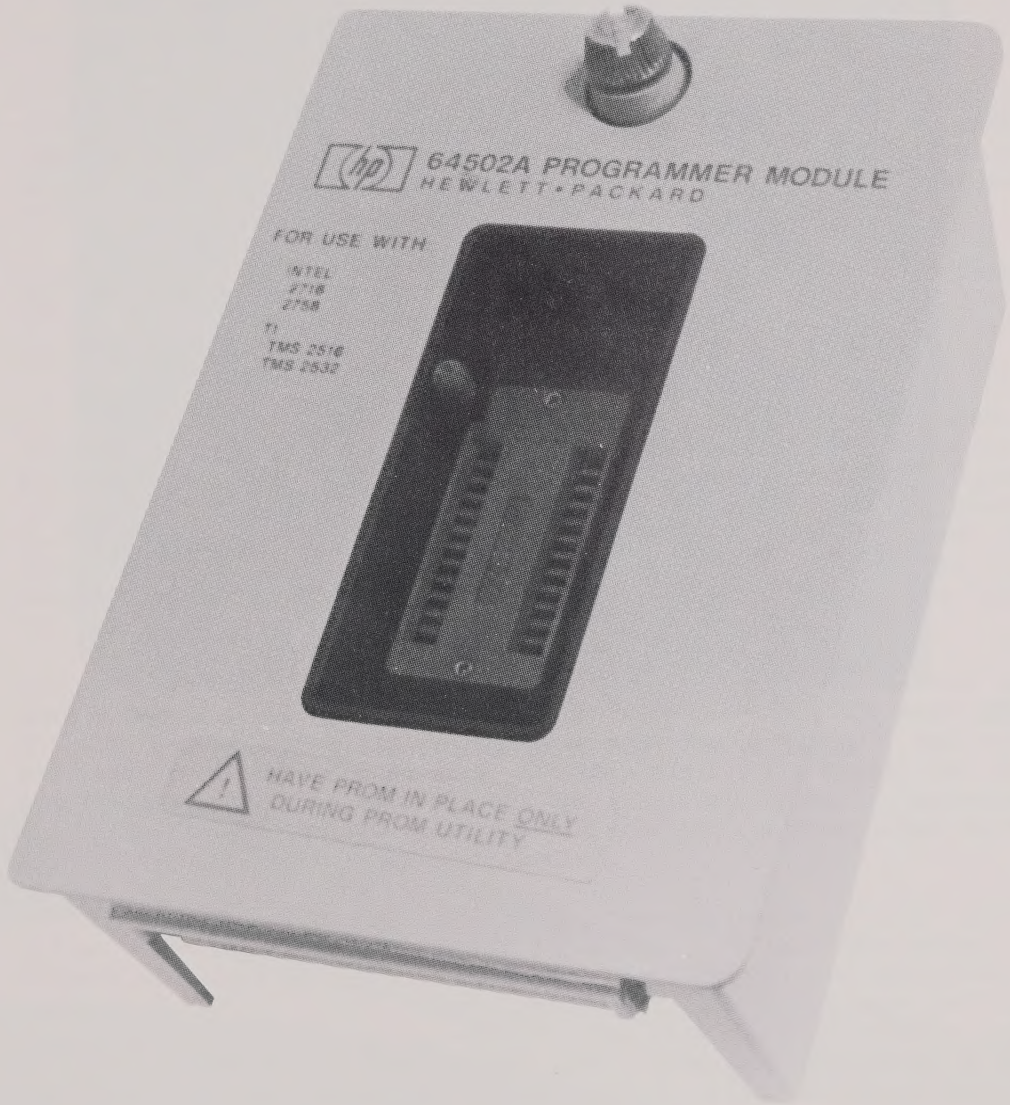
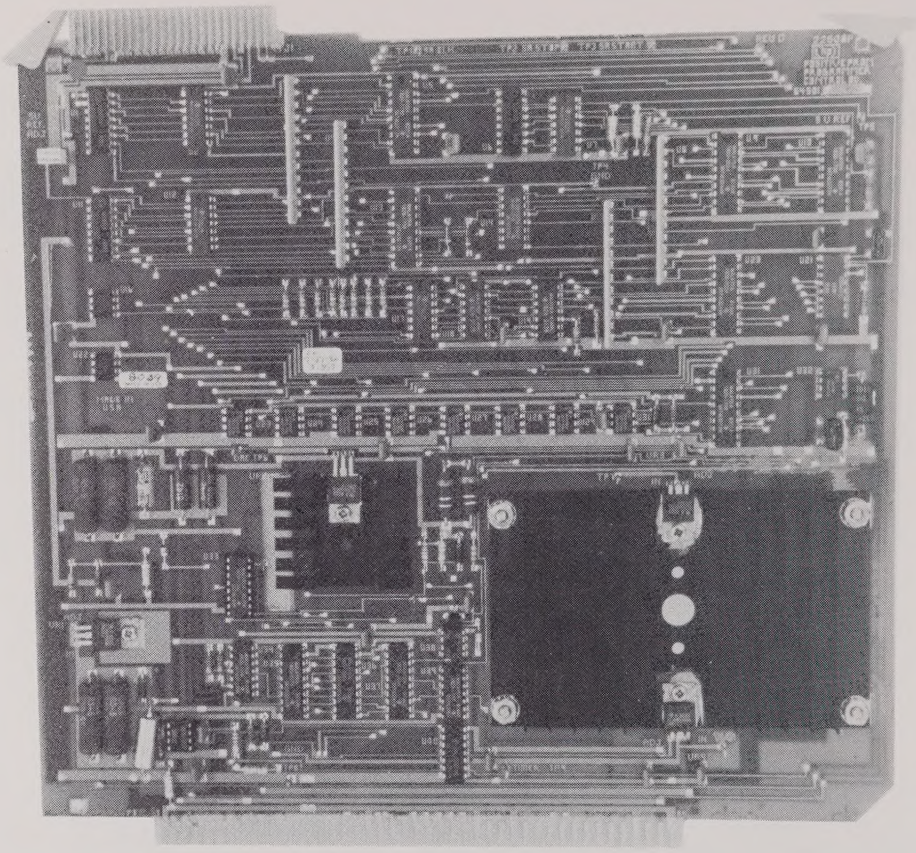


Model 64500S - 64502A Module

Figure 1-1. Model 64500S Prom Programmer Contents



Model 64500S PROM Programmer Control Board

Model 64500S Cable

Figure 1-1. Model 64500S Prom Programmer Contents (continued)

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual contains information required to install, test and service the Hewlett-Packard Model 64500S PROM Programmer. Operating instructions are provided in a seperate Operating Manual supplied with the instrument. It should be kept with the instrument for use by the operator.

1-3. Shown on the title page is a microfiche part number. This number can be used to order the microfilm transparencies of the manual.

1-4. INSTRUMENTS COVERED BY THIS MANUAL.

1-5. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last four are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-6. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument has been modified from those described in this manual. The manual for this modified instrument is accomplished by a Manual Change supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-7. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Change supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard Sales Service office.

1-8. For information concerning a repair number prefix that is not listed on the title page or in the Manual Change supplement, contact your nearest Hewlett-Packard Sales/Service Office.

1-9. DESCRIPTION.

1-10. The Hewlett-Packard Model 64500S Positive PROM Programmer is designed to program a wide variety of positive PROMs and EPROMs.

1-11. The Model 64500S consists of one Model 64501A Positive PROM Programmer and one or more programmer modules. One Model 64502A Programmer Module is supplied with every 64500S. Other programmer modules must be ordered seperately by model number, or by option as part of the Model 64500S.

1-12. Througout this manual the Positive PROM Programmer will be refered to as Model 64501A. It is the same as the Model 64500S except that the 64500S will have options included. The options are the programmer modules, i.e., Model 64503A, 64504A, 64505A, etc. The Model 64500S exists for marketing and ordering purposes. The service information for the programer modules is covered in the Service Manual for that module.

1-13. The PROM Programmer board may be ordered as Model 64501A. If the board is being ordered for replacement purposes, use the ten digit part number from the material list.

1-14. The Model 64502A is used for Positive PROM Programmer Performance Verification tests, and programming Intel's 2716 and 2758, Texas Instrument's TMS2516, and TMS2532 programable ROMs.

1-15. Pulse widths and sequences for the PROM being programmed are determined by the software.

1-16. Voltage levels, current levels, and rise or fall times are determined by the specific programmer hardware modules.

1-17. The Model 64500S performs the functions of read, write, and verification of programmable memories.

SECTION II

INSTALLATION AND REMOVAL

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the Model 64502A. Included are initial inspection procedures and instructions for repacking the instrument for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically. The electrical Procedures for checking Performance Verification are given in Section IV. If the contents are not complete, if there is mechanical damage or defect, or if the instrument does not pass the performance tests, notify the nearest Hewlett-Packard Sales/Service office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Sales/Service Office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP's option without waiting for claim settlement.

2-5. INSTALLATION PROCEDURE.

2-6. If the Positive PROM Programmer is installed in the Mainframe, it should be positioned in the front most unused connector. This is typically the fourth or fifth connector from the front of the Mainframe. The Input/Output Controller, Display Controller, and the CPU boards occupy the first three connectors respectively. The Floppy or Tape Controller board occupies the fourth connector when installed.

NOTE

The Model 64501A Positive PROM Programmer and programmer modules must be installed and removed with the mainframe's power turned off.

2-7. PROM PROGRAMMER CABLE.

2-8. A 50 conductor ribbon cable, W1, connects the PROM Programmer to the programmer module. The end of the cable with the single connector is connected to the top left corner of the PROM Programmer with the cable towards the front of the mainframe. The cable should be routed across the top of the card cage and down behind the front panel. The two connectors should be visible in the opening for the programmer module. Depending on the module being used, it can have one or two P.C. boards. If it has only one board, use the connector nearest the end of the cable. The P.C. boards and cable connectors are keyed so that they fit together only one way.

SECTION III

OPERATION

The operation of the PROM Programmer is a function of the system software. Complete operation from the keyboard of the system is beyond the scope of the Service Manual. Please refer to the Operator's Manual for the procedures.

CAUTION

The proper operation of the positive PROM programmer requires that a PROM be inserted ONLY AFTER the PROM programmer software module is called and that the PROM be REMOVED before the PROM programmer software module is exited.

NOTE

The PROM software module is called by pressing the "prom_prog" softkey then press the carraige return key. To exit the PROM programmer software module press the "end" softkey then press the carraige return key.

SECTION IV

PERFORMANCE VERIFICATION AND TROUBLESHOOTING

4-1. INTRODUCTION.

4-2. This section provides two types of performance tests: Operation Verification and Performance Verification. The Operation Verification provides approximately 90% assurance that the PROM Programmer and the 64502A Programmer Module are capable of programming a programmable ROM. The Performance Verification checks the electrical parameters of the PROM Programmer and the 64502A Programmer Module. Unless the detailed Performance Verification is required, we recommend that only the Operation Verification be performed.

4-3. EQUIPMENT REQUIRED.

4-4. No test equipment is required to perform the Operation Verification. However, the Performance Verification does require an Oscilloscope. Signature Analysis is not required for this Model.

4-5. The HP Model 64502A Programmer Module must be installed when running the Positive PROM Programmer Operation or Performance Verification. See the 64502A Service Manual for the installation procedure.

CAUTION

Model 64502A PROM Programmer Module is the only one that should be used when running the Operation or Performance Verifications. Other Modules can be permanently damaged.

4-6. If a problem does occur, refer to the Performance Verification theory for an understanding of its operation. This will help you in troubleshooting the PROM Programmer and the 64502A Programmer Module.

4-7. RUNNING THE OPERATION VERIFICATION.

a. Boot up the Operating System from the Disc. (See Operator's Manual for details).

b. From the Keyboard call up the PROM P.V. This is done by pressing the "opt_test" softkey, and then pressing the return key. When this is done, a table will be displayed indicating the location of the P.C. boards in the card cage of the mainframe. Press the number corresponding to the slot number which the PROM Controller PC board occupies. When this is done and the RETURN key is pressed, the PROM P.V. will be initated.

NOTE: The following softkeys should be displayed:

START CYCLE END TEST DAC=10V

c. Press the START softkey to run the Performance Verification and note the response. The test passes when the response "Digital Tests Passed" is displayed on the screen.

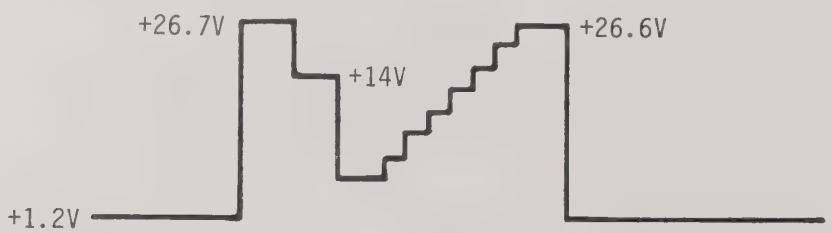
NOTE

The P.V. test is normally all that needs to be checked for a 90% confidence level. The following tests are normally performed by Service Personal.

4-8. RUNNING THE PERFORMANCE VERIFICATION.

a. Repeat the Operation Verification (Paragraph 4-7 steps a,b, and c).

b. Connect an oscilloscope to TP6 on the PROM Programmer board and note the following wave form:



The Waveform should be linear and the steps of equal size.

c. Monitor TP7 on the PROM Programmer board with an oscilloscope and note it is changing states during the Operation Verification test.

d. Momentarily touch a 50 ohm 5 watt wire wound resistor between pin 12 (ground) and pin 21 (DAC output) of the ZIF connector on the programmer module while in the start cycle, and note the test "DAC=26.7 V" fails. This checks the DAC'S overload circuits.

CAUTION

The resistor will get hot!
The DAC is capable of approx. 15 watts.

e. Press DAC=10 V and measure +9.9 V to +10.1 V at TP6 on the PROM Programmer board. See Section V if not within this range.

f. With an oscilloscope connected to TP9 on the Programmer board, press the END TEST softkey and observe that it changes states.

g. Connect the Reset Test Cable (from the Product Support Package Model 64932A) to connector J4 on the Input/Output board. Press the button on the cable and monitor U39 pin8 on the PROM Programmer board. The signal should switch from a high state to a low state (TTL Levels) each time the button is pressed.

4-9. PERFORMANCE VERIFICATION THEORY.

4-10. The Positive PROM Programmer Operation and Performance Verification includes about 50 individual tests of the digital circuits, and is initiated by pressing the START softkey. The tests are ordered in a manner that checks increasingly complex circuits. The tests also check the ability of the Digital to Analog Converter (DAC) to output its voltage range.

4-11. If all the tests pass, the DAC will generate a staircase ramp each time through the test sequence. Linearity of the ramp should be checked at TP6 with an oscilloscope.

4-12. If a failure is detected in the digital tests, the test sequence stops and an error message appears on screen. The message shows the expected inputs and outputs for the test failed.

4-13. Although all the bits are shown, with the most significant bit on the left, only those bits designated by a "L" or "H" are being checked in that test. Investigating the bits noted by an "L" or "H" will quickly locate the fault. When the status of all bits is not indicated, it implies that the unlisted bits are the complement of the listed bits.

4-14. Pressing START again will cause the test sequence to continue. The counter recording the number of tests failed will increment only once at the end of the sequence if a failure has been detected.

4-15. The CYCLE key allows the test sequence to run continuously without stopping when errors are detected. The number of tests and failures are counted by the counter recording that information. The error messages will write over any error messages existing from previous tests.

4-16. S/A is not used to troubleshoot the PROM programmers.

4-17. TROUBLESHOOTING USING PERFORMANCE VERIFICATION.

4-18. PROM Address.

4-19. The Positive PROM Programmer and the Self Test Programmer Module (Model 64502A) are discussed as being one unit since they will not work independently.

4-20. The signal names refer to the inputs/outputs between the PROM Programmer and the programmer module, not the interface to the Motherboard, e.g., CPU data becomes PROM address.

4-21. Tests 1 (HEX) through 17 (HEX) convert the data from the CPU to the address for the programmer module. The programmer module converts the addresss to I.D. codes which are returned to the PROM Programmer.

Table 4-1. Digital Tests of Address Lines

TEST#	NORMAL OUTPUTS U5 AND U13	NORMAL INPUTS U9	COMPONENTS TESTED
01	FFFF, CHECKS A12=1	11H10001	U36,13,9,14,33,35,37
02	FFFF, CHECKS A13=1	1H110001	U36,13,9,14,33,35,37
03	EFFF, CHECKS A12=1	11L10001	U36,13,9,14,33,35,37
04	DFFF, CHECKS A13=0	1L110001	U36,13,9,14,33,35,37
05	FFFF, CHECKS A14=1	1111000H	U22,VR4 (CHECK +40V)
06	BFFF, CHECKS A14=0	1111000L	U22,VR4 (CHECK +40V)
07	FFFF, CHECKS A15=1	111H0001	U13; U3 OF MODULE
08	FFFF, CHECKS MODULE	111HLLL1	U3,6,7 OF MODULE
09	7FFF, CHECKS A15=0 AND A0-A7=1	111L0101	U5; U3 OF MODULE
0A	7FFF, CHECKS DAC=+1.2V AND A8-A11,A14=1	111LLHL1	U5,VR3,U16; U3,6,7 OF MODULE
0B	7FFE, SETS A0=0	111HHHH1	TESTS ALL CICUITS ABOVE
0C	7FFD, SETS A1=0	111HHHL1	" " " " "
0D	7FFB, SETS A2=0	111HHLH1	" " " " "
0E	7FF7, SETS A3=0	111HHLL1	" " " " "
0F	7FEF, SETS A4=0	111HLHH1	" " " " "
10	7FDF, SETS A5=0	111HLHL1	" " " " "
11	7FBF, SETS A6=0	111HLLH1	" " " " "
12	7F7F, SETS A7=0	111HLLL1	" " " " "
13	7EFF, SETS A8=0	111LHHH1	" " " " "
14	7DFF, SETS A9=0	111LHHL1	" " " " "
15	7BFF, SETS A10=0	111LHLH1	" " " " "
16	77FF, SETS A11=0	111LHLL1	" " " " "
17	3FFF, SETS A14=0	111LLHH0	" " " " "

NOTE: DAC = +1.2V FOR ALL TESTS.

4-22. Table 4-1 displays the results of tests 1 (HEX) thru 17 (HEX). The CPU outputs a HEX address to the programmer module. When a test fails,that address will remain on U5 (lower byte) and U13 (upper byte) on the control board. That address causes the programmer module to return an ID code to U9, where:

U9=(XXXX)(XXXX)
Bit 7, U9 pin 11 Bit 0, U9 pin 2

Furthermore, when a failure is displayed, troubleshoot only the bits marked "H" or "L" on U9. These are the only bits examined by software. Therefore, it is possible to chase the failed bits with a logic probe because the PROM Programmer is not addressed after a failure. Note that tests 1 thru 4 check the control cicuitry on the PROM Control board and do not use the programmer module.

4-23. PROM Data.

4-24. Table 4-2 is a listing of read/write tests 18 (HEX) thru 27 (HEX) from the CPU. In each test, information is captured by the write data latches. This information is looped back through the module to the PROM Programmer and sent back to the CPU as read data, verifying continuity from the CPU to the PROM socket. The data returned to the CPU for verification is identical to that presented by the CPU for the test. Data is written to U31 where:

U31=(XXXX)(XXXX)
Bit 7, U31 pin 19 Bit 0,U31 pin 2

And is read at U20 where: U20=(XXXX)(XXXX)
Bit 7, U20 pin 11 Bit 0,U20 pin 2

Troubleshoot only the bits marked "H" or "L" of U20.

Table 4-2. Digital READ/WRITE Test

TEST	NORMAL OUTPUT U31	NORMAL INPUT U20	COMPONENTS TESTED
18	01, TEST DW0=1	0000000H	U31,20,19,30,14,33,35,37
19	FE, TEST DW0=0	1111111L	" " " "
1A	02, TEST DW1=1	000000H0	" " " "
1B	FD, TEST DW1=0	111111L1	" " " "
1C	04, TEST DW2=1	00000H00	" " " "
1D	FB, TEST DW2=0	11111L11	" " " "
1E	08, TEST DW3=1	0000H000	" " " "
1F	F7, TEST DW3=0	1111L111	" " " "
20	10, TEST DW4=1	000H0000	" " " "
21	EF, TEST DW4=0	111L0000	" " " "
22	20, TEST DW5=1	00H00000	" " " "
23	DF, TEST DW5=0	11L11111	" " " "
24	40, TEST DW6=1	0H000000	" " " "
25	BF, TEST DW6=0	1L111111	" " " "
26	80, TEST DW7=1	H0000000	" " " "
27	7F, TEST DW7=0	L1111111	" " " "

NOTE: DAC = +1.2V FOR ALL TESTS.

4-25. Digital to Analog Converter. (See Table 4-3.)

4-26. Test 28 (HEX) does not check anything. It is a delay preceding the Digital to Analog Converter tests.

4-27. Tests 29 (HEX) through 2D (HEX) check the Digital to Analog Converter (DAC).

4-28. Test 29 (HEX) sets the DAC to its lowest voltage.

4-29. Test 2A (HEX) checks the Current Sensor at the DAC's lowest voltage with a 50 ohm load.

4-30. Test 2B (HEX) checks the Current Sensor at the DAC's highest voltage, with a 50 ohm load. This insures the current sensing circuits will detect the current overload, and return the detection to the CPU.

4-31. Test 2C (HEX) sets the DAC's output to +14V. This is sent to the programmer module, is reduced through a voltage divider, sent to the Priority Encoders, and returned to the CPU via the I.D. codes and the data bus.

4-32. Test 2D (HEX) repeats Test 2C (HEX) except the voltage is decreased by .1 V.

4-33. Data is written to U10 where:

U10=(XXXX)(XXXX)
Bit 7, U10 pin 19 Bit 0, U10 pin 2

And read at U9 as an ID Code. The DAC output can be read at TP6.

Table 4-3. DAC Test

TEST#	NORMAL OUTPUT U10 AND TP6	NORMAL INPUT U9	COMPONENTS TESTEDltage
29	00, DAC=+1.2V	111LLHL1	U14,10,21,32,VR2
2A	00, DAC=+1.2V	H1100101	U38,Q1 PASSES WITH 50 OHM LOAD
2B	FF, DAC=+26.7V	H1100L11	U14,10,21,32,VR2,U38,Q1 TEST FAILS WITH 50 OHM LOAD
2C	80, DAC=+14.0V	H1100L11	U21,32,VR2
2D	7F, DAC=+13.9V	H1100L11	U21,32,VR2

NOTE: Address lines = 7FFF during DAC test.

SECTION V

ADJUSTMENT PROCEDURE

5-1. INTRODUCTION.

5-2. This section describes adjustments and checks required to return the +5 volt supply to operating capability after repairs have been made.

5-3. SAFETY REQUIREMENTS.

5-4. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summery at the front of this manual or with specific warnings given throughout the manual could result in serious injury or death. Service adjustments should be performed only by qualified service personnel.

5-5. EQUIPMENT REQUIRED.

5-6. A Voltmeter capable of .01 Volts D.C. accuracy is required for the Adjustment Procedure.

5-7. ADJUSTMENTS.

5-8. There is only one Adjustment on the Positive PROM Programmer Board.

5-9. +5 Volt Adjustment.

5-10. In order to adjust the +5 volt supply, the mainframe must be in the Operation Verification mode. Refer to page 4-1, paragraph 4-7, steps a and b.

5-11. Press the soft key labeled DAC=10 V, and adjust +5V REF, R36, for for +9.97V to +10.03V at the DAC output, TP6. Then check the voltage at TP5 for +4.65V to +5.3V.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one, all in capital letters; and two, partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Miscellaneous parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five-digit code that indicates the manufacturer of the part.

e. The manufacturer's part number.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlewtt-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/ Service Office.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-10. DIRECT MAIL ORDER SYSTEM.

6-11. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No Maximum or minimum on any mail order (there is a minimum order amount, for parts ordered through a local HP Office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-12. Mail-order forms and specific ordering information are available through your local HP Sales/Service Office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	assembly	F	fuse	MP	= mechanical part	U	integrated circuit
B	motor	FL	filter	P	= plug	V	= vacuum, tube, neon bulb, photocell, etc
BT	battery	IC	integrated circuit	Q	= transistor		
C	capacitor	J	jack	R	= resistor	VR	voltage regulator
CP	= coupler	K	relay	RT	= thermistor	W	cable
CR	diode	L	inductor	S	= switch	X	socket
DL	delay line	LS	loud speaker	T	= transformer	Y	crystal
DS	= device signaling (lamp)	M	meter	TB	= terminal board	Z	tuned cavity network
E	= misc electronic part	MK	microphone	TP	test point		

ABBREVIATIONS

A	= amperes	H	henries	N/O	= normally open	RMO	= rack mount only
AFC	automatic frequency control	HDW	= hardware	NOM	= nominal	RMS	root-mean square
AMPL	amplifier	HEX	hexagonal	NPO	= negative positive zero (zero temperature coefficient)	RWV	= reverse working voltage
		HG	mercury				
BFO	beat frequency oscillator	HR	= hour(s)				
BE CU	beryllium copper	HZ	hertz	NPN	= negative-positive-negative	S-B	slow-blow
BH	= binder head					SCR	screw
BP	bandpass			NRFR	= not recommended for field replacement	SE	= selenium
BRS	brass	IF	intermediate freq			SECT	section(s)
BWO	backward wave oscillator	IMPG	impregnated	NSR	= not separately replaceable	SEMICON	semiconductor
		INCD	incandescent			SI	silicon
CCW	counter-clockwise	INCL	include(s)			SIL	silver
CER	= ceramic	INS	insulation(ed)	OBD	= order by description	SL	= slide
CMO	= cabinet mount only	INT	= internal	OH	= oval head	SPG	= spring
COEF	coeficient			OX	= oxide	SPL	= special
COM	= common	K	kilo=1000			SST	stainless steel
COMP	= composition					SR	split ring
COMPL	= complete	LH	left hand	P	= peak	STL	steel
CONN	connector	LIN	linear taper	PC	= printed circuit		
CP	= cadmium plate	LK WASH	lock washer	PF	= picofarads= 10^{12} farads	TA	tantalum
CRT	= cathode-ray tube	LOG	logarithmic taper			TD	time delay
CW	= clockwise	LPF	low pass filter	PH BRZ	= phosphor bronze	TGL	toggle
				PHL	= phillips	THD	thread
DEPC	= deposited carbon	M	milli=10^{-3}	PIV	= peak inverse voltage	TI	titanium
DR	= drive	MEG	meg 10^{6}	PNP	= positive-negative-positive	TOL	tolerance
		MET FLM	metal film			TRIM	trimmer
ELECT	= electrolytic	MET OX	metallic oxide	P/O	= part of	TWT	traveling wave tube
ENCAP	= encapsulated	MFR	manufacturer	POLY	= polystyrene		
EXT	= external	MHZ	mega hertz	PORC	= porcelain	U	micro=10^{-6}
		MINAT	miniature	POS	= position(s)		
F	farads	MOM	momentary	POT	= potentiometer	VAR	= variable
FH	flat head	MOS	metal oxide substrate	PP	= peak-to-peak	VDCW	dc working volts
FIL H	= fillister head	MTG	mounting	PT	= point		
FXD	= fixed	MY	"mylar"	PWV	= peak working voltage	W/	= with
						W	watts
G	giga (10^{9})	N	nano (10^{-9})	RECT	rectifier	WIV	working inverse voltage
GE	germanium	N/C	normally closed	RF	= radio frequency		
GL	= glass	NE	neon	RH	= round head or right hand	WW	= wirewound
GRD	grounded	NI PL	nickel plate			W/O	without

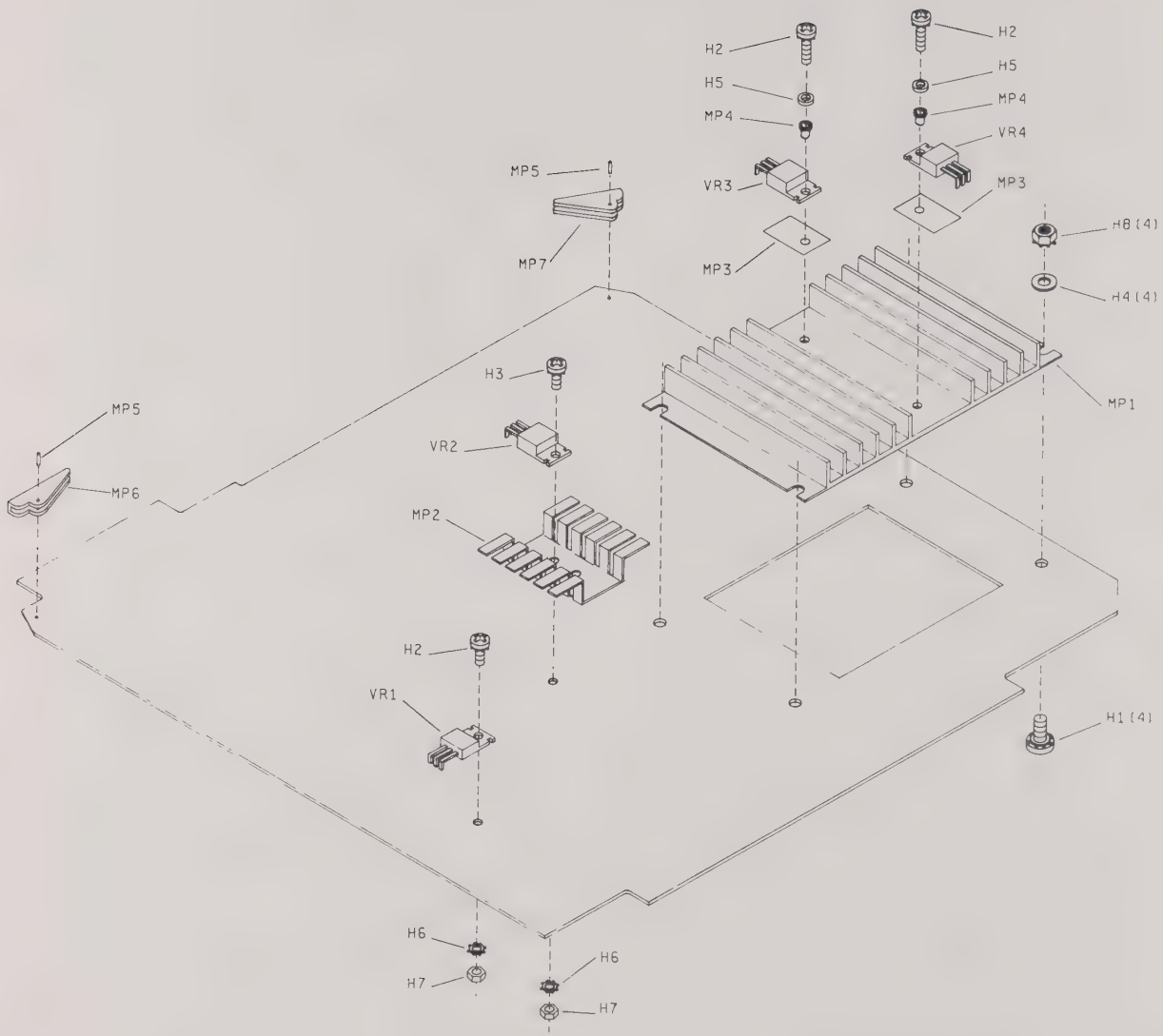


Figure 6-1. Illustrated Parts Breakdown

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64501-66502	0	1	BOARD ASSEMBLY, PROM PROGRAM	28480	64501-66502
C1	0160-3622	8	23	CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C2	0180-0230	0	6	CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
C3	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
C4	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C5	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C6	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C7	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C8	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C9	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C10	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C11	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C12	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C13	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C14	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C15	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C16	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C17	0180-1794	3	1	CAPACITOR-FXD 22UF+-10% 35VDC TA	56289	150D226X9035R2
C18	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C19	0180-0269	5	1	CAPACITOR-FXD 1UF+50-10% 150VDC AL	56289	30D105G150BA2
C20	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C21	0160-2207	3	1	CAPACITOR-FXD 300PF +-5% 300VDC MICA	28480	0160-2207
C22	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C23	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
C24	0140-0203	3	1	CAPACITOR-FXD 30PF +-5% 500VDC MICA	72136	DM15E300J050DMV1CR
C25	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
C26	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C27	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C28	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C29	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C30	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
C31	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C32	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
C33	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
H1	2360-0117	6	4	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H2	2200-0105	4	3	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H3	2200-0107	6	1	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H4	3050-0066	8	4	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0066
H5	3050-0235	3	2	WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
H6	2190-0005	0	2	WASHER-LK EXT T NO. 4 .116-IN-ID	28480	2190-0005
H7	2260-0001	5	2	NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK	28480	2260-0001
H8	2420-0001	5	4	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
MP1	1205-0380	6	1	HEAT SINK SPCL-HOLE-PATT	28480	1205-0380
MP2	1205-0376	0	1	HEAT SINK SGL PLSTC-PWR-CS	13103	60728
MP3	0340-0511	0	2	INSULATOR-XSTR KAPTON	28480	0340-0511
MP4	0340-0676	8	2	INSULATOR-FLG-BSHG NYLON	28480	0340-0676
MP5	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
MP6	64501-85002	6	1	EXTRACTOR, LEFT	28480	64501-85002
MP7	64501-85001	5	1	EXTRACTOR, RIGHT	28480	64501-85001
Q1	1854-0642	8	1	TRANSISTOR NPN SI PD=625MW FT=80MHZ	04713	MPS-A17
R1	0684-1511	0	2	RESISTOR 150 10% .25W FC TC=-400/+600	01121	CB1511
R2	0684-1511	0		RESISTOR 150 10% .25W FC TC=-400/+600	01121	CB1511
R3	0684-1021	7	3	RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R4	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R5	0683-5125	8	1	RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
R6	0683-1135	2	1	RESISTOR 11K 5% .25W FC TC=-400/+800	01121	CB1135
R7	0683-1845	1	8	RESISTOR 180K 5% .25W FC TC=-800/+900	01121	CB1845
R8	0683-1845	1		RESISTOR 180K 5% .25W FC TC=-800/+900	01121	CB1845
R9	0683-1845	1		RESISTOR 180K 5% .25W FC TC=-800/+900	01121	CB1845
R10	0683-1845	1		RESISTOR 180K 5% .25W FC TC=-800/+900	01121	CB1845
R11	0683-1845	1		RESISTOR 180K 5% .25W FC TC=-800/+900	01121	CB1845
R12	0683-1845	1		RESISTOR 180K 5% .25W FC TC=-800/+900	01121	CB1845
R13	0683-1845	1		RESISTOR 180K 5% .25W FC TC=-800/+900	01121	CB1845
R14	0683-1845	1		RESISTOR 180K 5% .25W FC TC=-800/+900	01121	CB1845
R15	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
R16	0698-3153	9	1	RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
R17	0698-3429	2	1	RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R18	0698-3634	1	2	RESISTOR 470 5% 2W MO TC=0+-200	28480	0698-3634
R19	0698-3634	1		RESISTOR 470 5% 2W MO TC=0+-200	28480	0698-3634
R20	0811-1200	5	2	RESISTOR .1 10% 2W PW TC=0+-800	75042	BWW2-2-1/10-K

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R21	0811-1200	5		RESISTOR .1 10% 2W PW TC=0+-800	75042	BWH2-2-1/10-K
R22	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R23	0811-1854	5	2	RESISTOR 50 5% 5W PW TC=0+-20	28480	0811-1854
R24	0811-1854	5		RESISTOR 50 5% 5W PW TC=0+-20	28480	0811-1854
R25	0698-3155	1	1	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R26	0811-2043	6	1	RESISTOR 12.71K .1% .25W PWW TC=0+-10	20940	143-1/8-E-12711-B
R27	0698-3239	2	1	RESISTOR 1.5K .25% .125W F TC=0+-50	28480	0698-3239
R28	0698-4055	2	1	RESISTOR 1K .25% .125W F TC=0+-100	03888	PME55-1/8-T0-1001-C
R29	0684-1021	1		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R30	0757-0403	2	3	RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
R31	0757-0403	2		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
R32	0811-1853	4	2	RESISTOR 25 5% 5W PW TC=0+-20	28480	0811-1853
R33	0811-1853	4		RESISTOR 25 5% 5W PW TC=0+-20	28480	0811-1853
R34	0757-0403	2		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
R35	0698-3445	2	1	RESISTOR 348 1% .125W F TC=0+-100	24546	C4-1/8-T0-348R-F
R36	2100-2520	9	1	RESISTOR-TRMR 50 20% C SIDE-ADJ 1-TRN	30983	ET50X500
TP1-TP10	0360-0535	0	10	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1810-0301	4	3	NETWORK-RES 16-DIP$1.0 OHM X 8	01121	3168$10
U2	1906-0074	1	4	DIODE-ARRAY 50V 400MA	28480	1906-0074
U3	1810-0049	7	4	NETWORK-RES 12-SIP6.8K OHM X 10	28480	1810-0049
U4	1810-0049	7		NETWORK-RES 12-SIP6.8K OHM X 10	28480	1810-0049
U5	1820-1730	6	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U6	1810-0301	4		NETWORK-RES 16-DIP$1.0 OHM X 8	01121	3168$10
U7	1906-0074	1		DIODE-ARRAY 50V 400MA	28480	1906-0074
U8	1810-0049	7		NETWORK-RES 12-SIP6.8K OHM X 10	28480	1810-0049
U9	1820-2024	3	3	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U10	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U11	1810-0301	4		NETWORK-RES 16-DIP$1.0 OHM X 8	01121	3168$10
U12	1906-0074	1		DIODE-ARRAY 50V 400MA	28480	1906-0074
U13	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U14	1820-1240	3	2	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U15	1810-0049	7		NETWORK-RES 12-SIP6.8K OHM X 10	28480	1810-0049
U16	1820-2207	4	2	IC DRVR TTL AND DUAL	01295	SN75471P
U17	1906-0074	1		DIODE-ARRAY 50V 400MA	28480	1906-0074
U18	1826-0138	8	2	IC COMPARATOR GP QUAD 14-DIP-P	04713	MLM339P
U19	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP-P	04713	MLM339P
U20	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U21	1826-0188	8	1	IC CONV 8-B-D/A 16-DIP-C	04713	MC1408L-8
U22	1820-2207	4		IC DRVR TTL AND DUAL	01295	SN75471P
U23	1820-2044	7	8	IC DRVR TTL AND DUAL 2-INP	01295	SN75461P
U24	1820-2044	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75461P
U25	1820-2044	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75461P
U26	1820-2044	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75461P
U27	1820-2044	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75461P
U28	1820-2044	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75461P
U29	1820-2044	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75461P
U30	1820-2044	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75461P
U31	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U32	1826-0207	2	1	IC OP AMP WB 8-DIP-P	27014	LM318N
U33	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U34	1820-1568	8	1	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
U35	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
U36	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U37	1820-1624	7	1	IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U38	1826-0412	1	1	IC COMPARATOR PRCN 8-DIP-P	01295	LM393
U39	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U40	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U41	1826-0180	0	1	IC TIMER TTL MONO/ASTBL	04713	MC1455P1
VR1	1826-0393	7	4	LM317T	27014	LM317T
VR2	1826-0393	7		LM317T	27014	LM317T
VR3	1826-0393	7		LM317T	27014	LM317T
VR4	1826-0393	7		LM317T	27014	LM317T
VR5	1902-0074	3	1	DIODE-ZNR 7.15V 5% DO-7 PD=.4W TC=+.047%	28480	1902-0074
VR6	1902-3172	8	1	DIODE-ZNR 11V 2% DO-7 PD=.4W TC=+.062%	28480	1902-3172
W1	8120-3346	7	1	CABLE, POSITIVE PROM	28480	8120-3346
				MISCELLANEOUS PARTS		
XU39	7120-6492	9	1	LABEL WARNING	28480	7120-6492
XU41	1200-0607	8	1	SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0607

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
00466	NORELCO NORTH AMER PHILIPS LTG CORP	LOS ANGELES	CA	90021
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
01928	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	08876
03888	KDI PYROFILM CORP	WHIPPANY	NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
09023	CORNELL-DUBILIER ELEK DIV FED PAC	SANFORD	NC	27330
13103	THERMALLOY CO	DALLAS	TX	75234
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
20940	MICRO-OHM CORP	EL MONTE	CA	91731
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
26654	VARADYNE INC	SANTA MONICA	CA	90404
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
27777	VARO SEMICONDUCTOR INC	GARLAND	TX	75040
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
30983	MEPCO/ELECTRA CORP	SAN DIEGO	CA	92121
32997	BOURNS INC TRIMPOT PROD DIV	RIVERSIDE	CA	92507
34333	MOTOROLA INC	FRANKLIN PARK	IL	60131
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
71590	CENTRALAB ELEK DIV GLOBE-UNION INC	MILWAUKEE	WI	53201
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108
75382	KULKA ELECTRIC CORP	MT VERNON	NY	10550
75915	LITTELFUSE INC	DES PLAINES	IL	60016

See introduction to this section for ordering information

SECTION VII

MANUAL BACKDATING

This section contains information for adapting this manual to the 64500S with serial prefix number 1924A that have a 64501-66501 board installed.

CHANGE 1

Page 6-5, table 6-2,
Change: The 64501-66502 board to 64501-66501, CD=0.

Page 8-11, figure 8-2,
Change: Replace schematic with the one attached in this section.

NOTE: The board and schematic will have to be modified. The correct ID (1000H) is not always transmitted on the 64501-66501 board due to the internal bus on the board floating when the ID is read. This usually occurs when other options are installed. Refer to Service Note 65500S-2.

Page 7-3/(7-4 blank) shows the alterations to fix the ID problem.

A 64000 system with the card cage heavily loaded may cause the Model 64501A Prom Programmer Controller to transmit an incorrect ID Code when the option-test softkey is pressed. As a result, the Prom Programmer will not be recognized.

This note applies only to the 64501-66501 circuit card. This problem has been corrected on the 64501-66502 circuit card, serial prefix 2239A.

MODIFICATION INSTRUCTIONS:

1. Remove U33 and solder socket XU33, Part No. 1200-0607, in place.
   Add this 16-pin IC socket to the parts list of the 64500S.

2. Cut traces to pins 15 and 6 as shown in figure 1.

3. Cut trace to U33 pin 1 as shown in Figure 2. Add jumpers from from U33 pins 1. 6 and 14 to feedthrough holes as shown in Figure 2.

4. Replace U33.

5. Update the Prom Programmer schematic as shown in Figure 3 and check out the circuits which were modified for shorts & continuity.

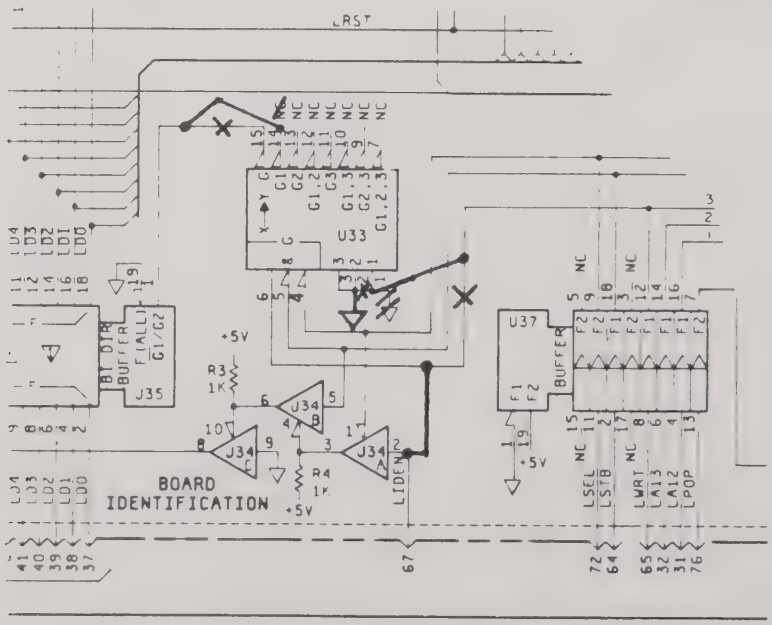
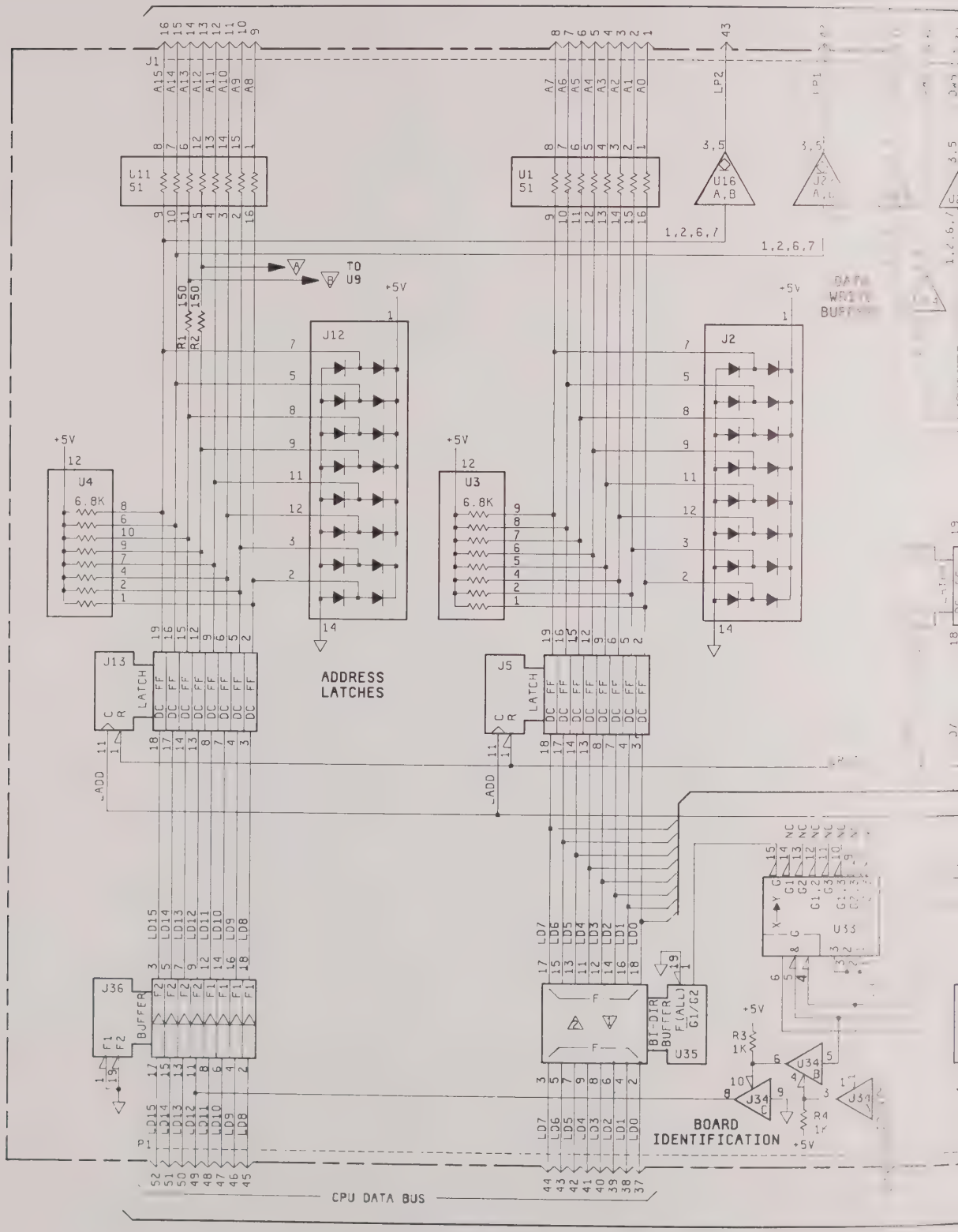
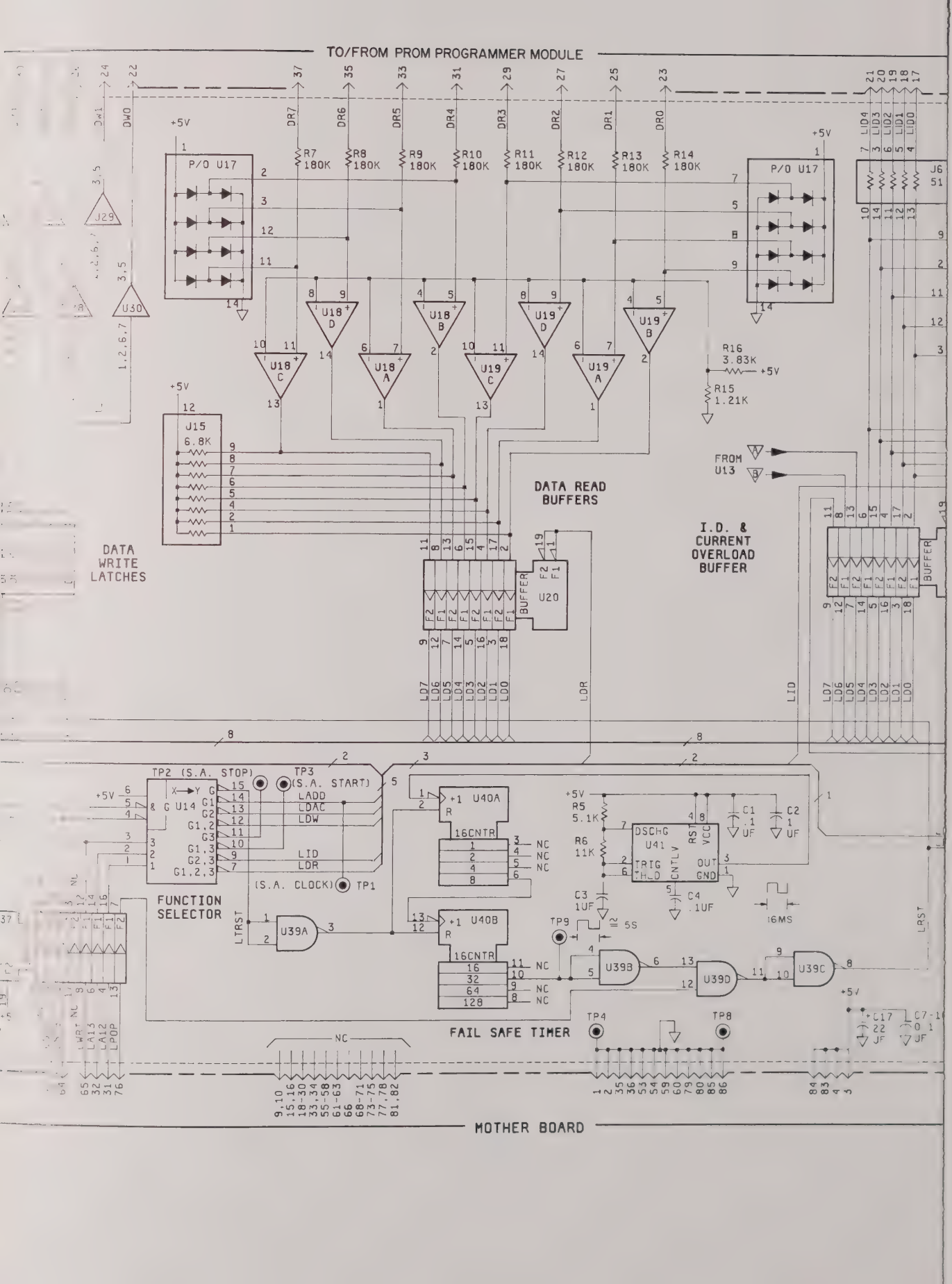
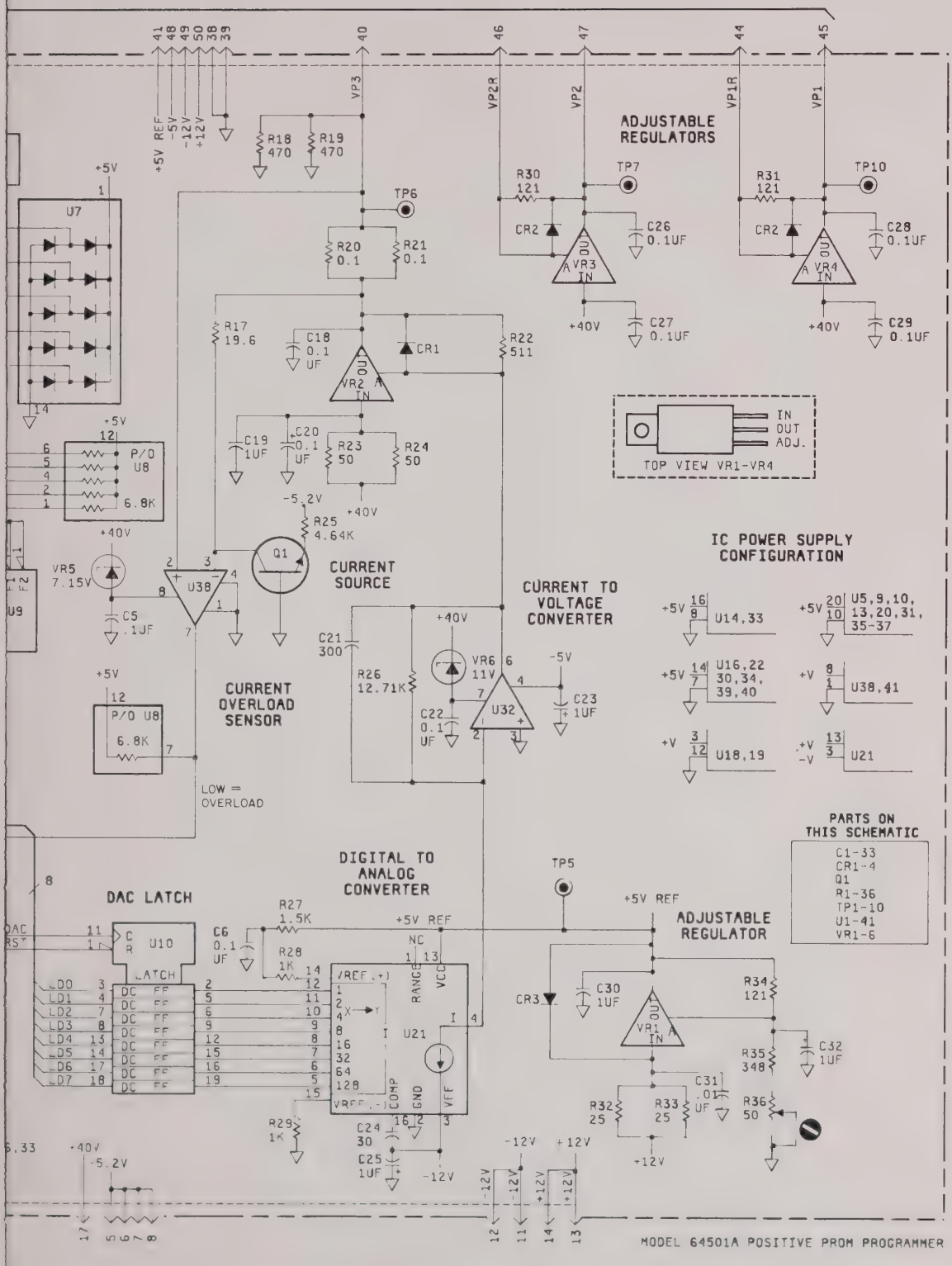


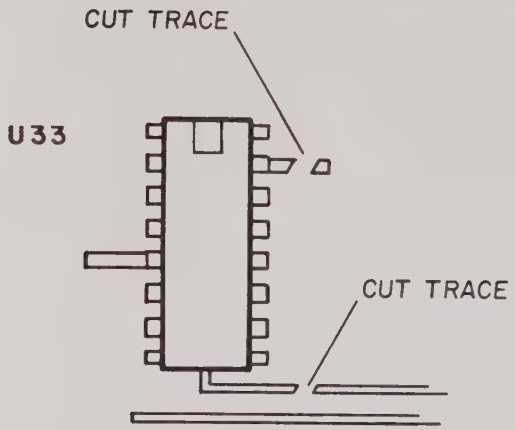
Figure 7-2. Modifying the 64501-66501 board


J1
A15 A14 A13 A12 A11 A10 A9 A8
A7 A6 A5 A4 A3 A2 A1 A0
LP2
U11
51
U1
51
U16
A,B
1,2,6,7
TO
U9
+5V
R1 150
R2 150
J12
J2
U4
6.8K
U3
6.8K
J13
LATCH
J5
LATCH
ADDRESS
LATCHES
_ADD
LD15 LD14 LD13 LD12 LD11 LD10 LD9 LD8
LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0
J36
BUFFER
F1
F2
BI-DIR
BUFFER
F(ALL)
G1/G2
U35
U33
R3
1K
R4
J34
BOARD
IDENTIFICATION
P1
CPU DATA BUS

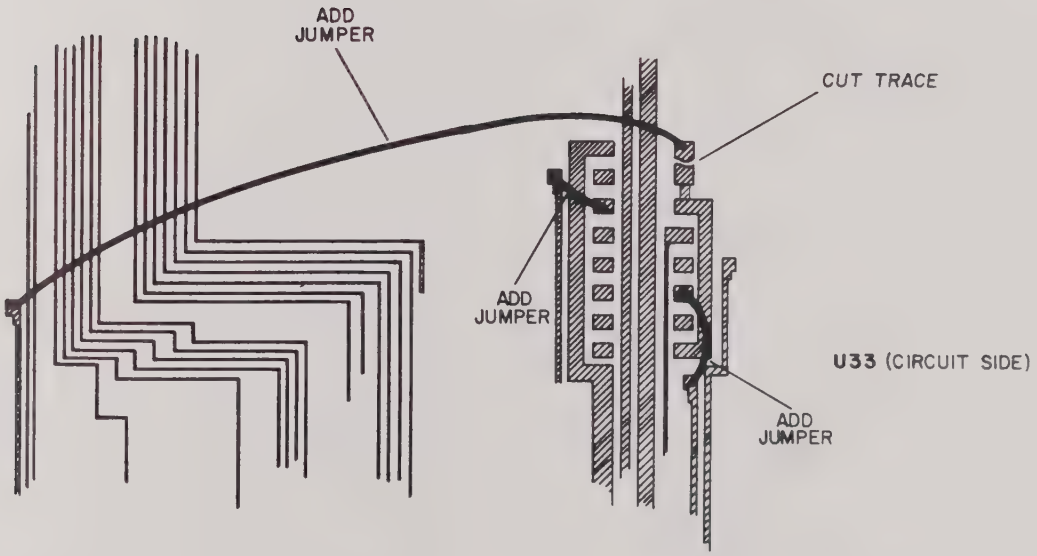

TO/FROM PROM PROGRAMMER MODULE
+5V
P/O U17
R7 180K
R8 180K
R9 180K
R10 180K
R11 180K
R12 180K
R13 180K
R14 180K
U18 D
U18 B
U19 D
U19 B
U18 C
U18 A
U19 C
U19 A
R16 3.83K
R15 1.21K
J15 6.8K
DATA WRITE LATCHES
DATA READ BUFFERS
I.D. & CURRENT OVERLOAD BUFFER
FROM U13
U20
BUFFER
LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0
LDR
LID
TP2 (S.A. STOP)
TP3 (S.A. START)
LADD
LDAC
LDW
LID
LDR
(S.A. CLOCK)
TP1
FUNCTION SELECTOR
U14
U40A
U40B
16CNTR
U39A
U39B
U39C
U39D
U41
DSCHG
TRIG
THLD
CNTLV
RST
VCC
OUT
GND
R5 5.1K
R6 11K
C1 .1 UF
C2 1 UF
C3 1UF
C4 .1UF
16MS
TP9
TP4
TP8
FAIL SAFE TIMER
LTRST
LRST
NC
MOTHER BOARD



MANUAL BACKDATING Figure 8-2.
Prom Programmer Controller Schematic
64501-66501
Page 8-11
PROM Prog 7-3



Component Side 64501-66501



Circuit Side 64501-66501

Figure 7-3. Schematic Changes to the 64501-66501 board

SECTION VIII

THEORY AND SCHEMATICS

8-1. INTRODUCTION.

8-2. This section contains information for troubleshooting and repairing the Model 64501A PROM Programmer.

8-3. The block diagram, schematic, component locator, and other service information are provided on fold-out service sheets to help you in servicing the Model 64501A PROM Programmer. Table 8-1 Logic Symbology will aid you in reading and interpreting the new Logic Symbols.

8-4. BLOCK DIAGRAM THEORY.

8-5. Buffers U35, U36 and U37 are drivers that buffer the Positive PROM Programmer from the CPU Bus.

8-6. Function Selector U14 controls the various functions on the Positive PROM Programmer. U33 determines which direction data will flow through U35.

8-7. U39, U40, and U41 form a Timer to prevent over heating of the Programmer's components if the CPU program fails to operate properly.

8-8. U16 and U22 are used to develop pulses and voltages required to program the PROM.

8-9. U34 developes the board I.D. of the Positive PROM Programmer Identification Code.

8-10. Socket ID and Current Overload Buffer U9 returns the Programmer Module's Identification Code and Current Overload Status to the CPU.

8-11. DAC Latch U10, DAC U21, Current to Voltage Converter U32, and Adjustable Regulators VR1 and VR2, form a programmable voltage source. The range is +1.2 V to +26.7 V in .1 volt steps.

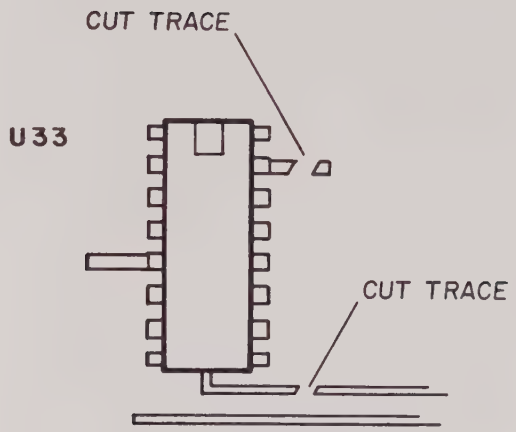
8-12. U38 is a current overload sensor.

8-13. VR3 and VR4 are Adjustable Voltage Regulators.

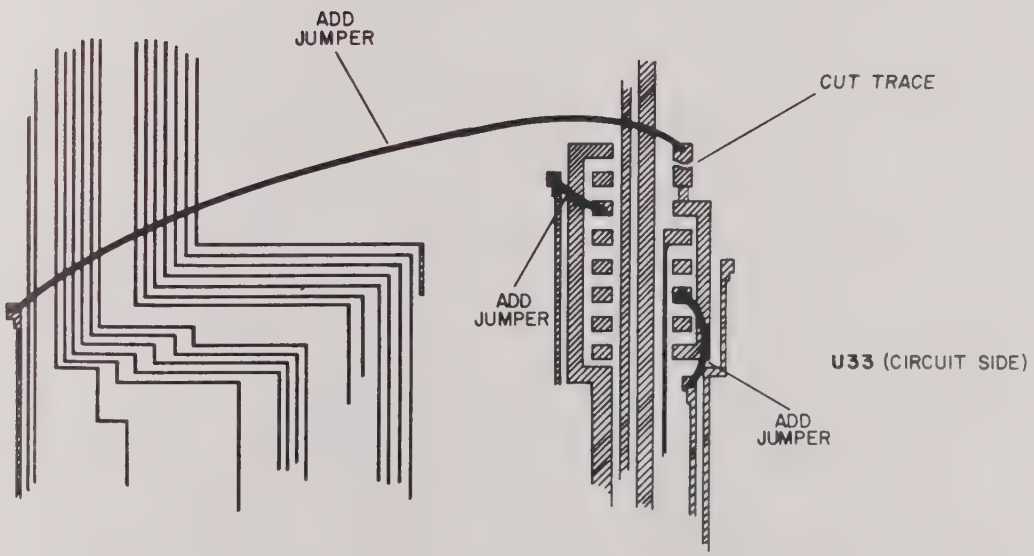
8-14. Address Latches U5 and U13 develop the PROM's address.

8-15. Data Write Buffers U23 through U31 write the data to the PROM being programmed.

8-16. Data Read Buffers U18, U19, and U20 return the data read from the PROM to the CPU for verificaton.



Component Side 64501-66501



Circuit Side 64501-66501

Figure 7-3. Schematic Changes to the 64501-66501 board

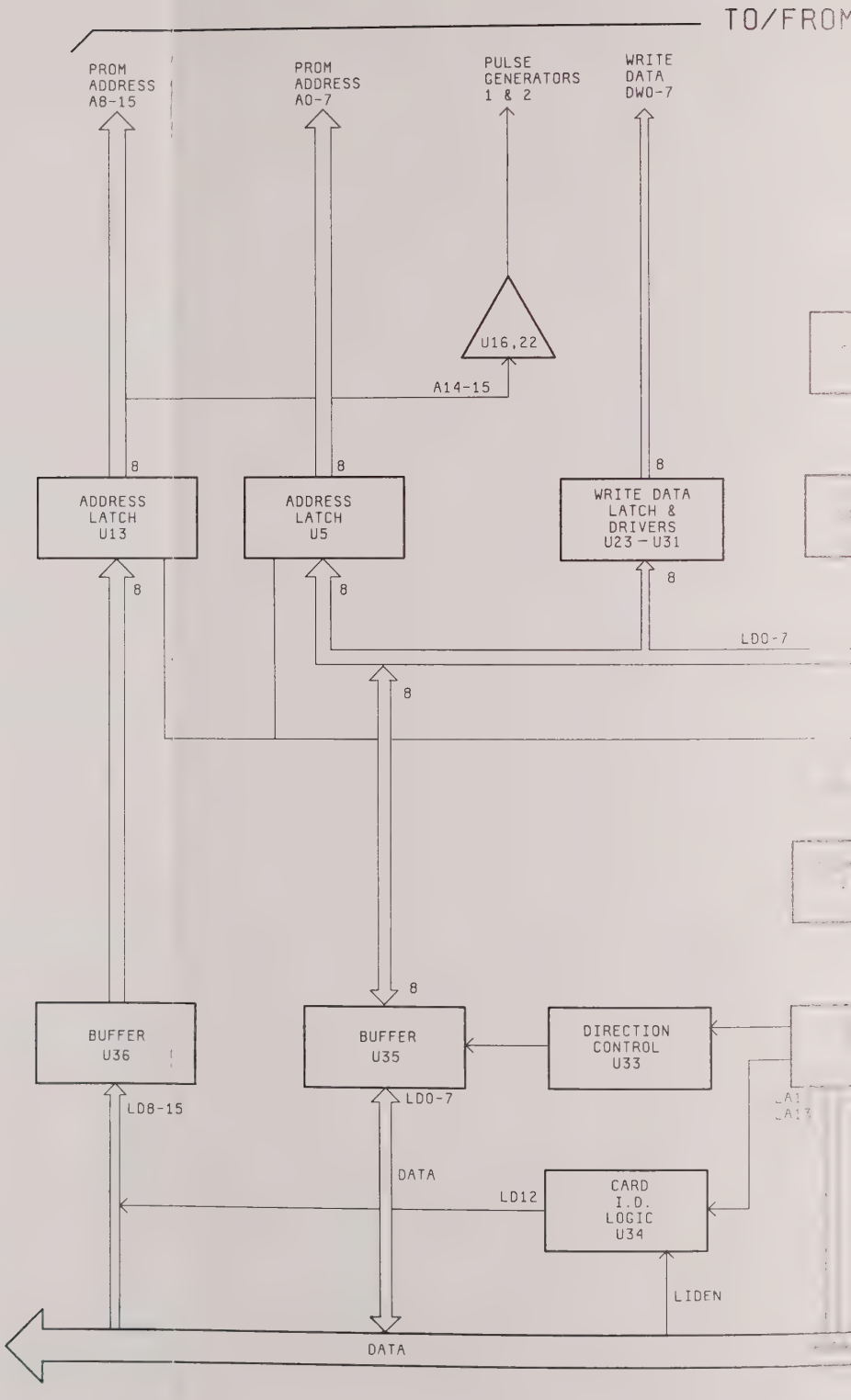
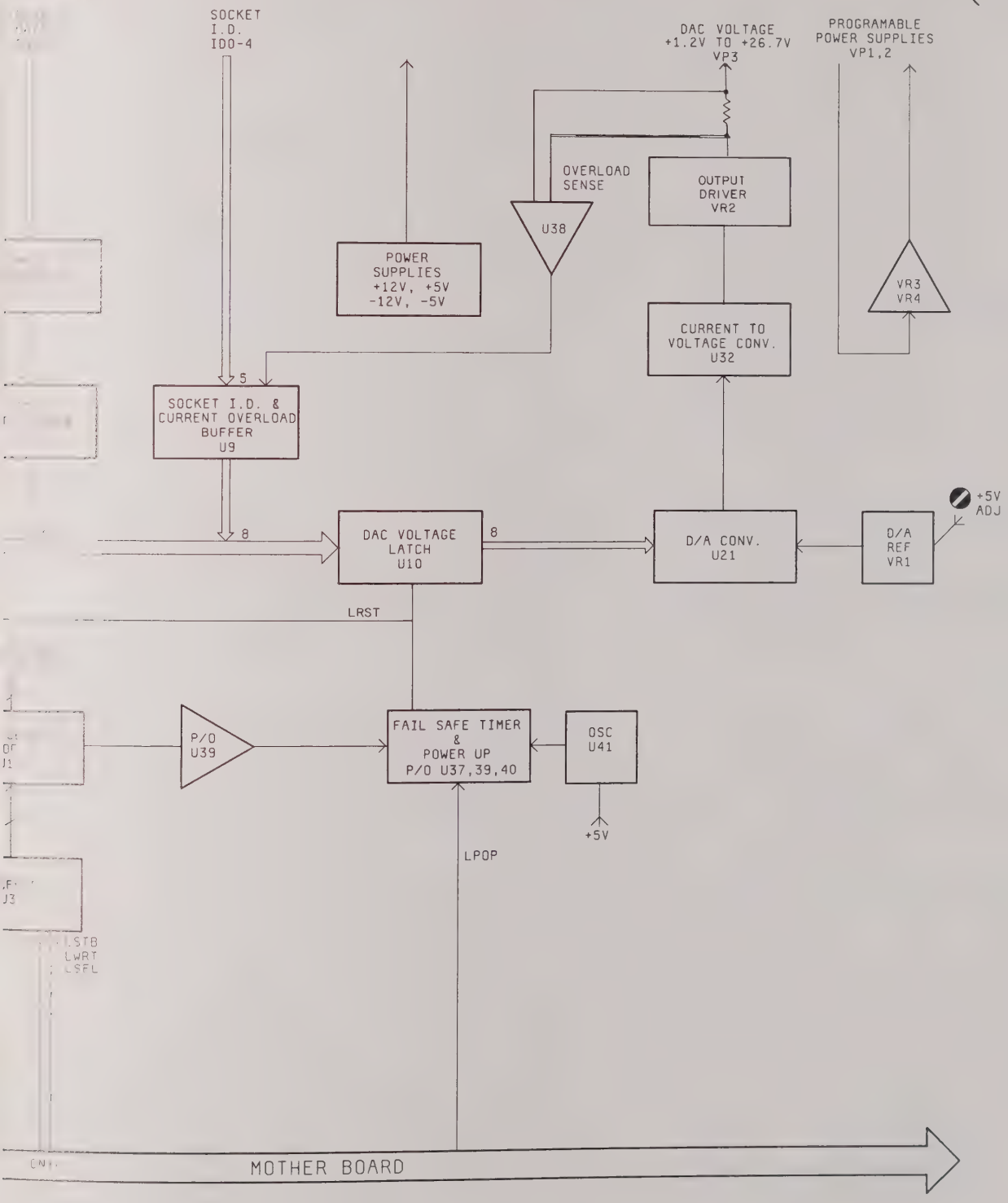


Figure 8-1.
Block Diagram
PROM Prog 8-2

PROM PROGRAMMER MODULES



64501A POSITIVE PROM PROGRAMMER DRIVER

SECTION VIII

THEORY AND SCHEMATICS

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8-13. VR3 and VR4 are Adjustable Voltage Regulators.

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8-15. Data Write Buffers U23 through U31 write the data to the PROM being programmed.

8-16. Data Read Buffers U18, U19, and U20 return the data read from the PROM to the CPU for verificaton.

Table 8-1. Logic Symbology

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, an
outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term

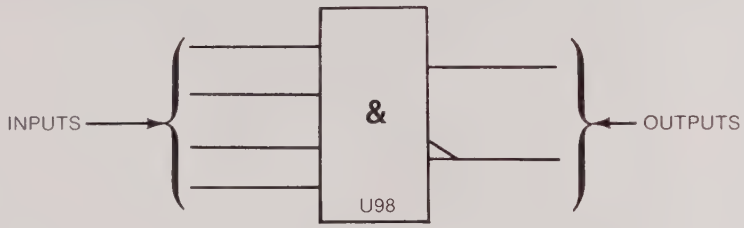
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

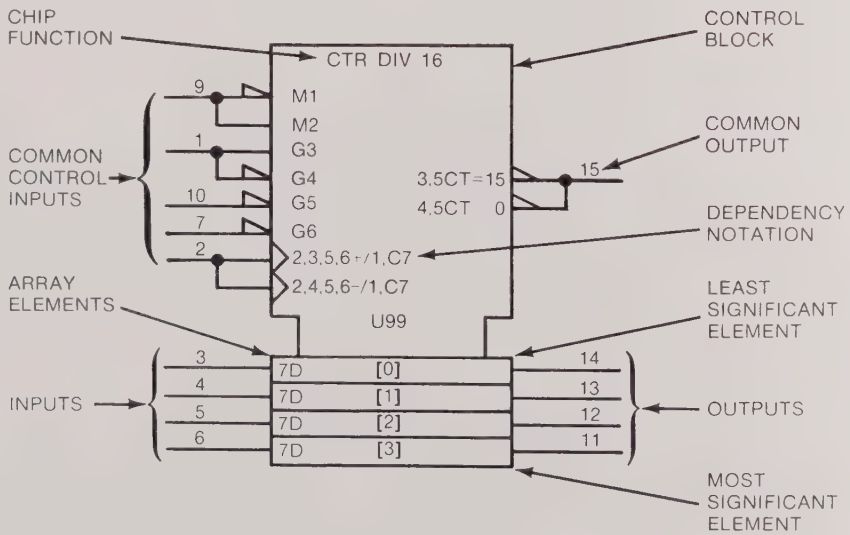
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and
representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs
located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation
Any array element is independent of all other array elements. Unless indicated, the least significant element is alway
closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powe
of 2 (shown in **[ ]**).

Table 8-1. Logic Symbology (cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

LS-08-09-82 - 2

8-24. Positive PROM Programmer Identification.

8-25. When the CPU forces LIDEN, LSEL, and LSTB low, and the Positive PROM Programmer is present in the mainframe, a low state on LD12 is developed by board I.D. U34. (Pull-up resistors on the CPU data bus pull other data lines high.) EFFF HEX is returned to the CPU on the data bus. If FFFF HEX is returned, the CPU will not allow Positive PROM Programming.

8-26. Programmer Module Identification.

8-27. Programmer module identification code is developed on the module's P.C. board. The I.D. code is generated by grounding combinations of lines ID0 through ID4, A12, and A13 in the programmer module. A12 and A13 are shared between PROM address and I.D. code. R1 and R2 allow the programmer module to pull A12 and A13 low for the I.D. code without damaging the outputs of Address Latch U13, even if they are high.

8-28. The I.D. code is buffered by I.D. and Current Overload Buffer U9, and is returned through U35 when requested by the CPU. The CPU uses the I.D. code to determine which PROMs may be programmed in the module installed in the mainframe. The unique code for each module may be found in the theory of operation for the programmer modules.

8-29. Programmable Positive Power Supply.

8-30. After the PROM is installed, the CPU programs power supply VP3 and checks the power being used by the PROM. The DAC Latch U10 latches digital information from the CPU for the Digital to Analog Converter, U21. DAC U21 is refernced to +5 V supplied by an adjustable regulator, VR1. DAC U21 converts the 8 bit digital word to a programmed current level that drives the Voltage to Current Converter U32.

8-31. U32 is a current to voltage converter referenced to +29 V. Depending on the current from the the DAC U21 the output voltage will range from approximately 0 V to +25.5 V. With the 8 bit resolution of U21, the output of U32 will have a resolution of .1 V.

8-32. Adjustable Regulator VR2 is referenced to +40 V allowing the output to "follow" the Voltage to Current Converter U32. VR2's output is always +1.2 V greater than U32's output. Therefore, the output of VR2 will vary from +1.2 V to +26.7 V in .1 V steps (U21's input: 00 HEX=+1.2 V, FF HEX=+26.7 V). R23 and R24 share power disipation with VR2.

Table 8-1. Logic Symbology (cont'd)

OTHER SYMBOLS

Analog Signal	Inversion	Shift Right (or down)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
Bit Grouping	Nonlogic Input/Output	▽ Tri-State
Buffer	Open Circuit (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	Open Circuit (external resistor)	( ) Used for factoring terms using algebraic techniques.
Dynamic	≥1 OR	[ ] Information not defined.
=1 Exclusive OR	Passive Pull Down (internal resistor)	Φ Logic symbol not defined due to complexity.
Hysteresis	Passive Pull Up (internal resistor)	
? Interrogation	Postponed	
— Internal Connection	← Shift Left (or up)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	-	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

	Astable
	Delay
	Nonretriggerable Monostable
NV	Nonvolatile
	Retriggerable Monostable

8-17. THEORY OF OPERATION.

8-18. General.

a. The theory of the Positive PROM Progrmmer is discussed in the order of events as they occur under software control.

b. The Positive PROM Programmer communicates with the CPU over the CPU data bus. Only two address lines are used, LA12 and LA13.

c. The addresses for the PROM being programmed are developed on the Positive PROM Programmer P.C. board.

d. U35 buffers the lower eight bits of the CPU data bus. Control lines LWRT, LSEL, and LSTB from the CPU in conjunction with U33 determine if U35 is in the send or receive mode.

e. U36 buffers the upper eight bits of the CPU data bus, and is receive only on the Positive PROM Programmer.

f. U37 buffers CPU control lines LSTB, LWRT, LA12, LA13, LSEL LPOP.

g. Function Selector U14 decodes LA12, LA13, and LWRT to control data flow on the Positive PROM Programmer.

8-19. DETAILED THEORY.

8-20. Fail Safe Timer.

8-21. U39, 40, and U41 form a "Fail-Safe Timer" that uses the output of U41 as the clock. Normally the timer is reset by the software at least every 100 milliseconds. If the program fails to execute properly or some other failure occurs, the timer will not be reset and will count all 32 states (approx 500 milliseconds). This forces U39 pin 8 low, clearing the Adrress Latches U5 and U13, DAC Latch U10, and Data Write Latch U31.

8-22. Pulse Generators.

8-23. U16 and U22 are dual positive AND drivers. There are two sections of each I.C. which are connected in parallel to provide 500 milliamps of current sinking ability. The two signals developed by the CPU (LD14,15) are used to generate pulses and voltage levels of different values. The different values can be found in the theory of operation for each of the programmer modules.

8-24. Positive PROM Programmer Identification.

8-25. When the CPU forces LIDEN, LSEL, and LSTB low, and the Positive PROM Programmer is present in the mainframe, a low state on LD12 is developed by board I.D. U34. (Pull-up resistors on the CPU data bus pull other data lines high.) EFFF HEX is returned to the CPU on the data bus. If FFFF HEX is returned, the CPU will not allow Positive PROM Programming.

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8-29. Programmable Positive Power Supply.

8-30. After the PROM is installed, the CPU programs power supply VP3 and checks the power being used by the PROM. The DAC Latch U10 latches digital information from the CPU for the Digital to Analog Converter, U21. DAC U21 is refernced to +5 V supplied by an adjustable regulator, VR1. DAC U21 converts the 8 bit digital word to a programmed current level that drives the Voltage to Current Converter U32.

8-31. U32 is a current to voltage converter referenced to +29 V. Depending on the current from the the DAC U21 the output voltage will range from approximately 0 V to +25.5 V. With the 8 bit resolution of U21, the output of U32 will have a resolution of .1 V.

8-32. Adjustable Regulator VR2 is referenced to +40 V allowing the output to "follow" the Voltage to Current Converter U32. VR2's output is always +1.2 V greater than U32's output. Therefore, the output of VR2 will vary from +1.2 V to +26.7 V in .1 V steps (U21's input: 00 HEX=+1.2 V, FF HEX=+26.7 V). R23 and R24 share power disipation with VR2.

8-33. Current Sensor.

8-34. R20 and R21 are current sensing resistors that develop a voltage proportional to the current being drawn by the PROM. R18 and R19 are load resistors for VR2 when there is no PROM in the module's socket.

8-35. Current Source Q1 developes 20 millivolt accross R17 with 1 milliamp of current. R17's 20 millivolt in addition to the voltage developed accross R20 and R21, with no load, will keep U38's output in the high state. This indicates to the CPU that less than 400 milliamps is being drawn from VR2.

8-36. When current through R20 and R21 is greater than 400 milliamps, the voltage accross R20 and R21 becomes great enough to offset the 20 millivolts accross R17. When this happens, the output of U38 goes to a low state indicating to the CPU that an overload condition exists. The CPU then programs the Power Supply to +1.2 V until the overload is removed.

8-37. Adjustable Voltage Sources.

8-38. VR3 and VR4 are adjustable regulators that are referenced by the programmer module. The voltages are different for the various modules and may be found in the theory of operation for the programmer modules. The outputs are +1.2 V more positive than the adjustment inputs.

8-39. POSITIVE PROM PROGRAMMING (not operation).

8-40. The sequence of events is different for the various PROMs and will not be presented in detail here. For detailed information see the appropriate manufacturer's data sheets for the PROM being programmed.

8-41. U5 and U13 latch the address to the PROM being programmed. The address is clocked into the filp-flops by U14 when directed by the CPU. They will be cleared in the event of any power-up sequence by LPOP, or by the Fail-Safe Timer.

8-42. U31 latches the data to be written to the PROM being programmed. The data is clocked into the flip-flops by U14 when directed by the CPU. They will be cleared in the event of any power up sequence by LPOP, or by the Fail-Safe Timer.

8-43. Data Write Buffers U23 through U30 are dual positive AND drivers. Each section of the drivers can sink about 250 milliamps. Both sections are connected in parallel to allow sinking of 500 milliamps. The PROM data write lines are connected in different ways for each programmer module, and is discussed in detail in the theory of operation for each module.

8-44. PROM DATA VERIFICATION.

8-45. Durind the programming sequence, information is burned into the PROM and then read. This read is a dummy read and nothing is verified. The actual read/verify occurs after the PROM has been completely programmed. After the PROM is programmed, the information in the PROM is read and compared to the information in the user file. If an error occurs during the verification then an error message appears on the screen.

8-46. Verification is done through Data Read Buffers U18 and U19. U18 and U19 provide a high impedance input for the PROM. U18 and U19 are made TTL compatable by R15 and R16, setting the input threshold to +1.2 V. Resistor Package U15 pulls the comparators up for the inputs of the Data Read Buffers U20.

8-47. When requested by the CPU, through Function Selector U14 (LDR), the data will be returned to the CPU for verification via U20 and U35.

8-48. Signals in the PROM Programmer have been assigned Mnemonics that describe the active state and function of the signal line. Mnemonic functional definitions are listed alphabetically in Table 8-2.

Table 8-2. PROM Programmer Mnemonics

Mnemonic	Description
A0-15	Address 0 through 15 -- these sixteen address lines are sent to the Programmer Module from the PROM Programmer. Some or all of them may be used to program a PROM. They are derived from the data sent to the PROM Programmer over the CPU Data Bus (LD0-15) by the CPU.
DR0-7	Data Read 0 through 7 -- these data lines are used to read the data contents of a programmed PROM. The data read is sent to the CPU over the CPU Data Bus for verification. Some or all of these lines may be used.
DW0-7	Data Write 0 through 7 -- these data lines are used to write data to the PROM being programmed. The data sent to the PROM is derived from the information sent over the CPU Data Bus by the CPU. Some or all of these lines may be used.
LID0-4	Low Identification 0 through 4 -- these five lines are used to return Identification Codes from the Programmer Modules to the CPU over the CPU Data Bus. By returning an ID Code,the CPU can determine which Programmer Module is installed, and therefore, can tell the operator via the CRT which PROMs may be programmed.
LA12-13	Low Address 12 and 13 -- two of sixteen address lines from the Address Bus (P/O CPU Bus) used to select different functions on the PROM Programmer.
LADD	Low Address -- when low, allows the information on the CPU Data Bus to be latched into the Address Latches. From the outputs of these two Latches, the information becomes the address for the PROM being programmed.
LD0-15	Low Data 0 through 15 -- a 16 bit bidirectional bus that is part of the CPU Bus.
LDAC	Low Digital to Analog Converter -- when low, allows the CPU's Data Bus information to be latched into the DAC Latch, setting the voltage at TP6 (VP3).
LDR	Low Data Read -- when low, allows the data read from the programmed PROM to be returned to the CPU for verification.

Table 8-2. PROM Programmer Mnemonics (Cont'd)

Mnemonic	Description
LDW	Low Data Write -- when low, allows the CPU's Data Bus information to be latched into the Data Write Latch. The outputs of the Latch become the Data to be written to the PROM being programmed.
LID	Low Identification -- when low, allows the Identification Code from the Programmer Module to be buffered by the I.D. and Current Sense Buffer, and returned to the CPU over the CPU's Data Bus. Current Overload Status is also sent to the CPU at this time.
LIDEN	Low Identification Enable -- when low along with LSEL, and LSTB, LD12 will go low. When LD12 is low and the other Data Lines are high, the CPU will recognize that there is a Positive PROM Programmer installed in the Mainframe's Card Cage.
LP1-2	Low Program 1 and 2 -- these two lines are used in conjunction with VP1 and VP2 to develope the various voltages and waveforms used to program PROMs. Sometimes LP1 and/or LP2 are looped back from the Programmer Module to VP1 and/or VP2.
LPOP	Low Power On Pulse -- resets all latches on the PROM Control Board, so that power dissiapation is minimum. LPOP will override the Timer in the event of an A.C. Power transient. When low, causes LRST to go low.
LRST	Low Reset -- when low, LRST will reset both Address Latches, the Data Write Latch, and the DAC Latch. Reseting these Latches causes the Address to be 0000 HEX with 00 HEX being the Data written, and the lowest power dissipation possible in the PROM being programmed.
LSEL	Low Select -- when low, anable the CPU to interact with the Prom Programmer. The CPU can write to (LWRT low), read (LWRT high), or read ID (LIDEN low) from the Prom Programmer.

Table 8-2. PROM Programmer Mnemonics (Cont'd)

Mnemonic	Description
LSTB	Low Strobe -- when LSTB and LWRT are both low, the CPU is writing to a device over the CPU's Data Bus. If LSEL is also low, the PROM Programmer will recieve the information. If LSEL is high, the PROM Programmer will not pay attention to the information sent on the bus. If LSTB is low, and LWRT is high, and the PROM Programmer is selected (LSEL low), then the PROM Programmer will return information to the CPU over the CPU's Data Bus.
LTRST	Low Timer Reset -- Resets the failsafe timer when low.
LWRT	Low Write -- when low, indicates the CPU is writing to the addressed device.
VP1-2	Voltage, Programmable 1 and 2 -- Adjustable Regulators used for developing various voltages and waveforms used for programming PROMs. The adjustable inputs (VP1R and VP2R) can be connected to LP1 and LP2 or to voltage dividers located on the Programmer Modules.
VP1R, VP2R	Voltage, Programmable Regulated -- Inputs to VR3 and VR4 which program thier outputs to +1.2 volts above VP1R and VP2R respectively.
VP3	Voltage, Programmable 3 -- Output of voltage regulator VR2 used for developing various voltage levels used for programming PROMs. VP3 is under program control due to DAC U21.

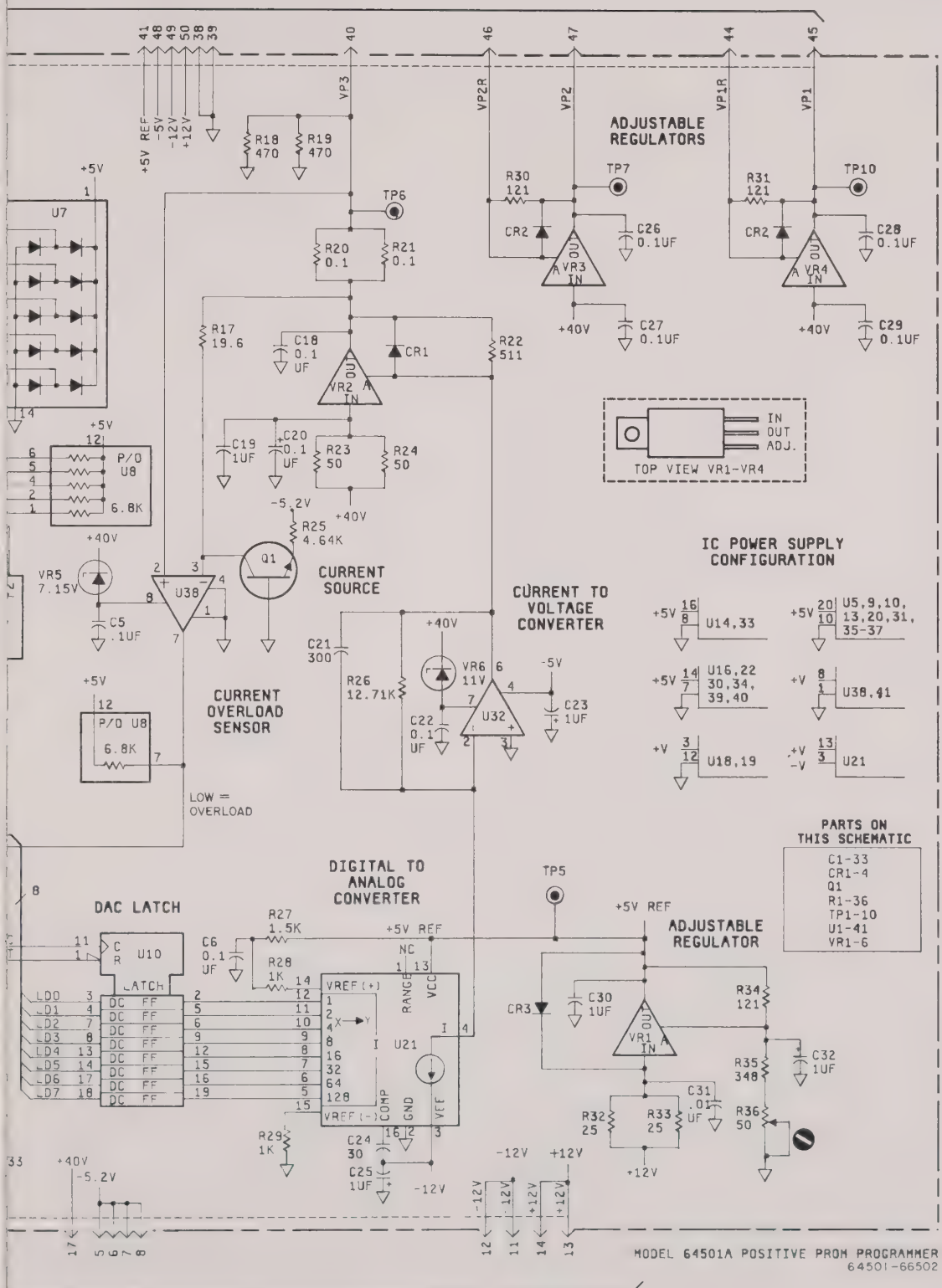
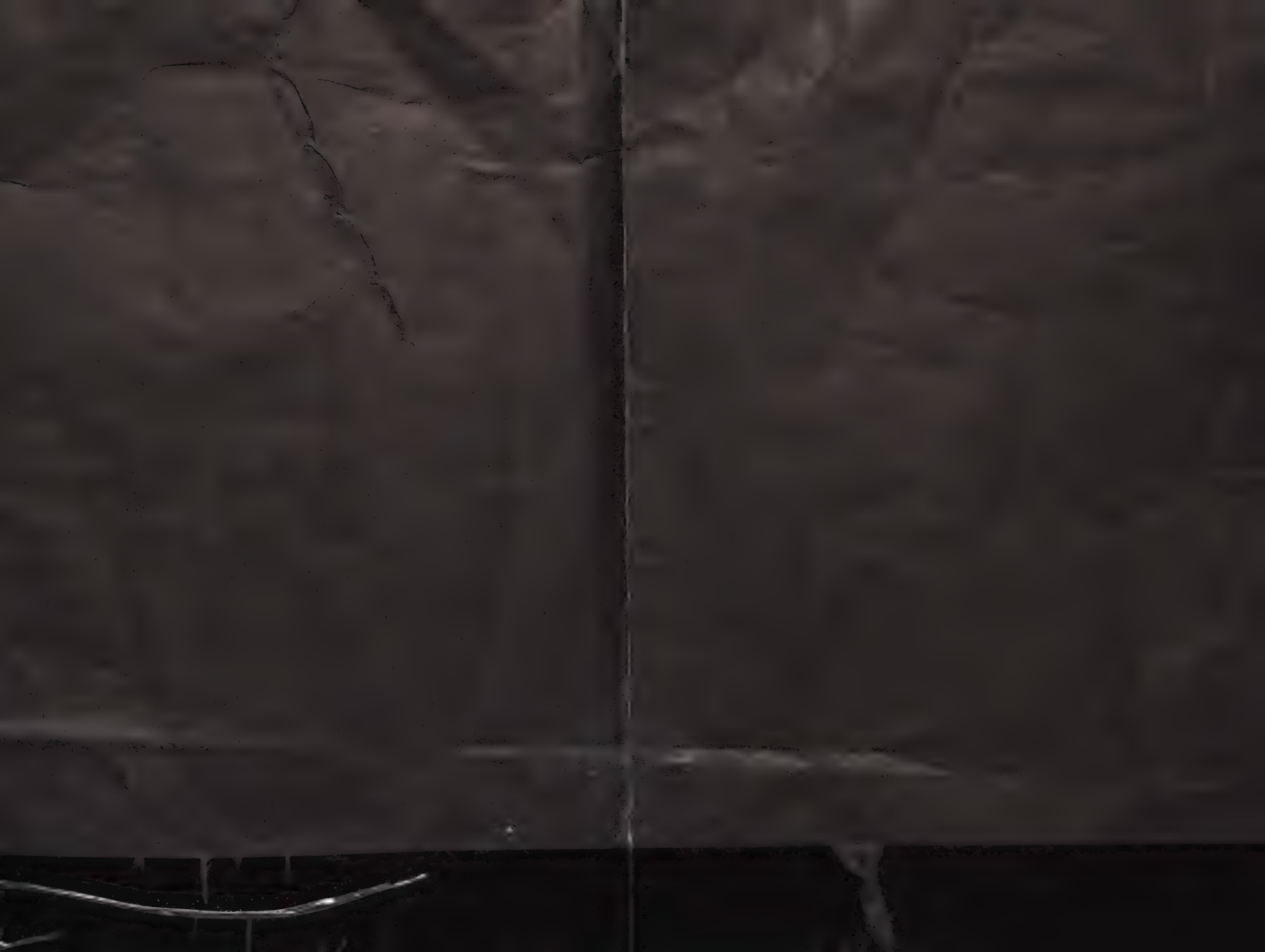
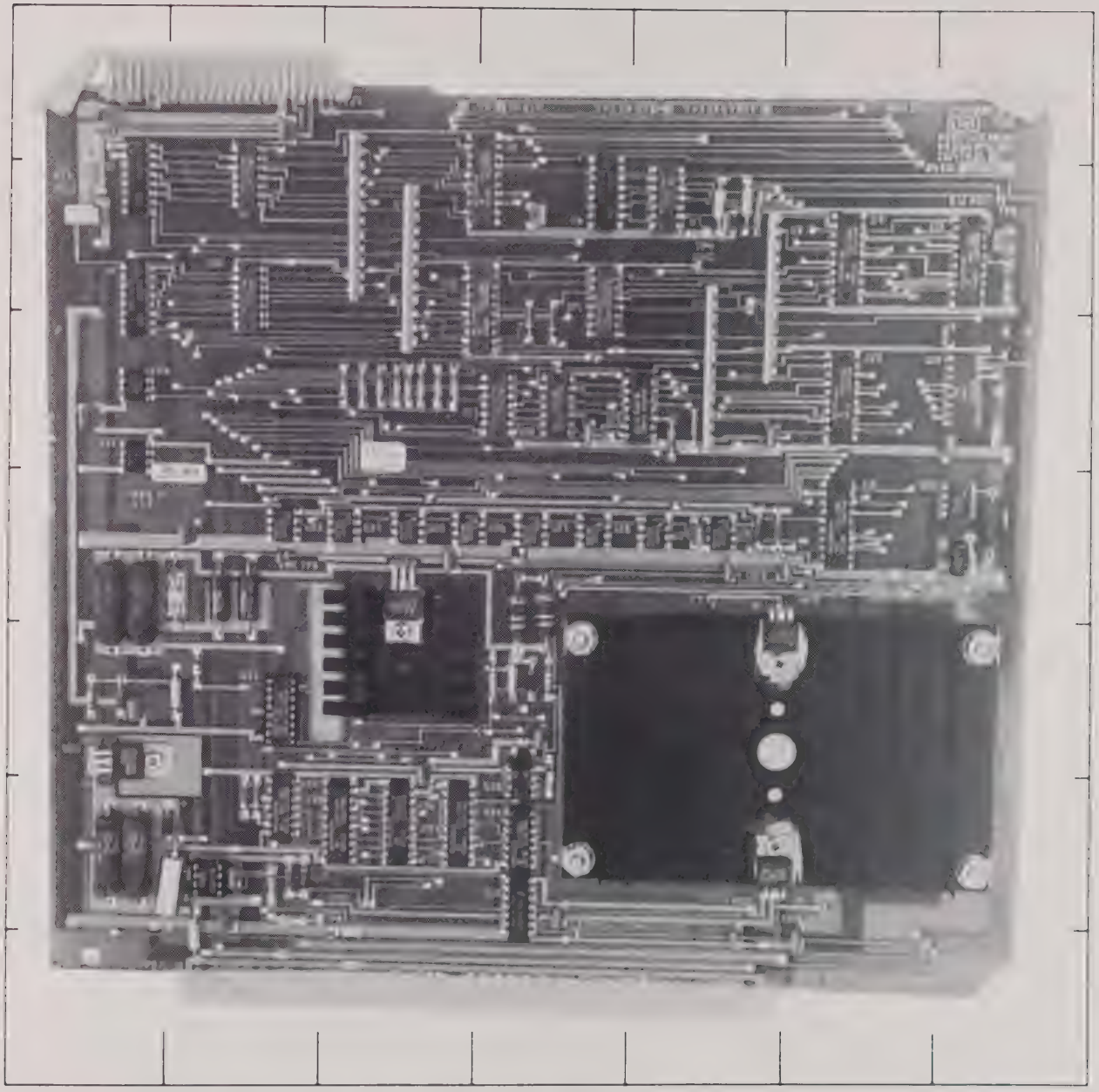


Figure 8-2.
PROM Programmer
PROM Prog 8-11

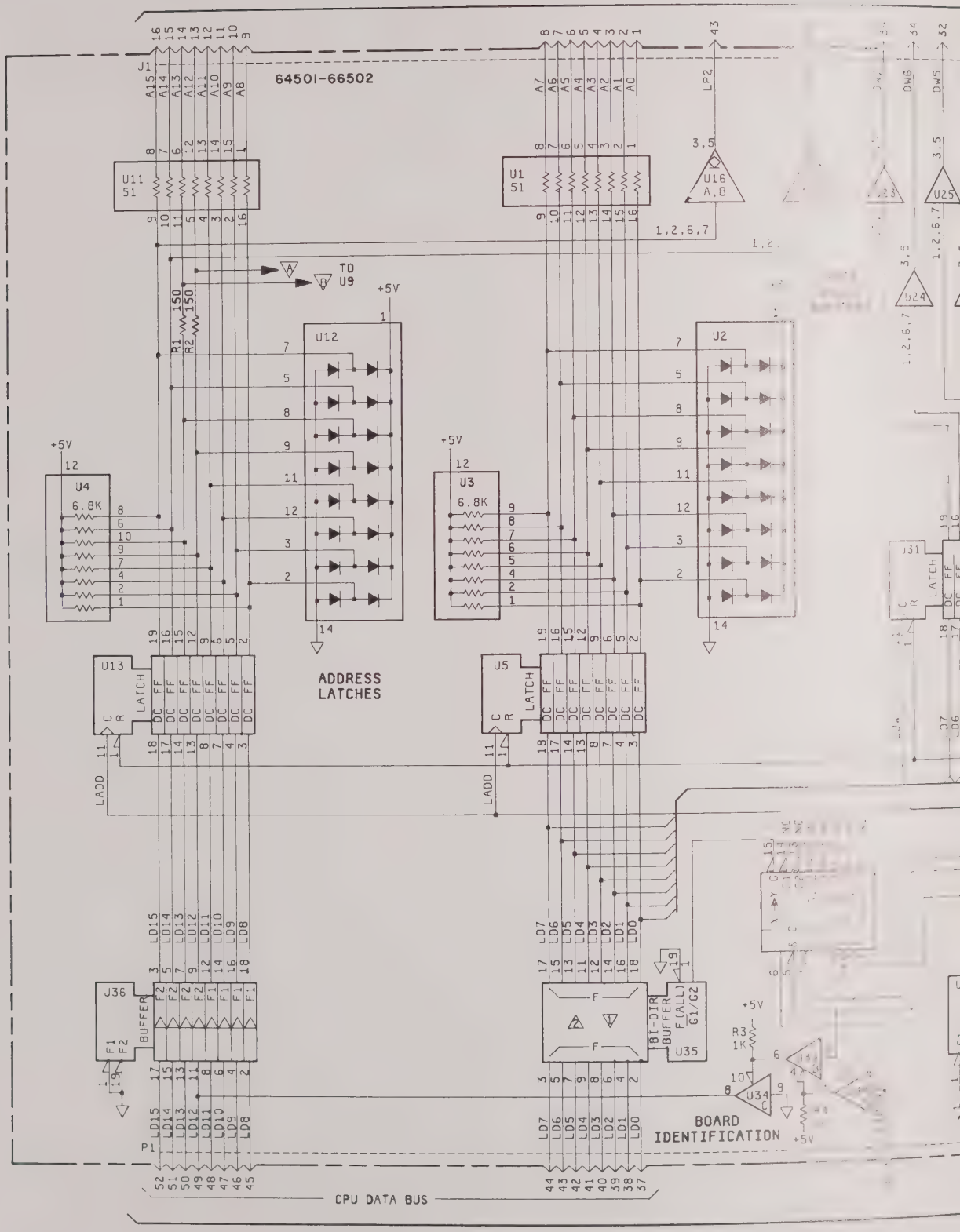
Table 8-2. PROM Programmer Mnemonics (Cont'd)

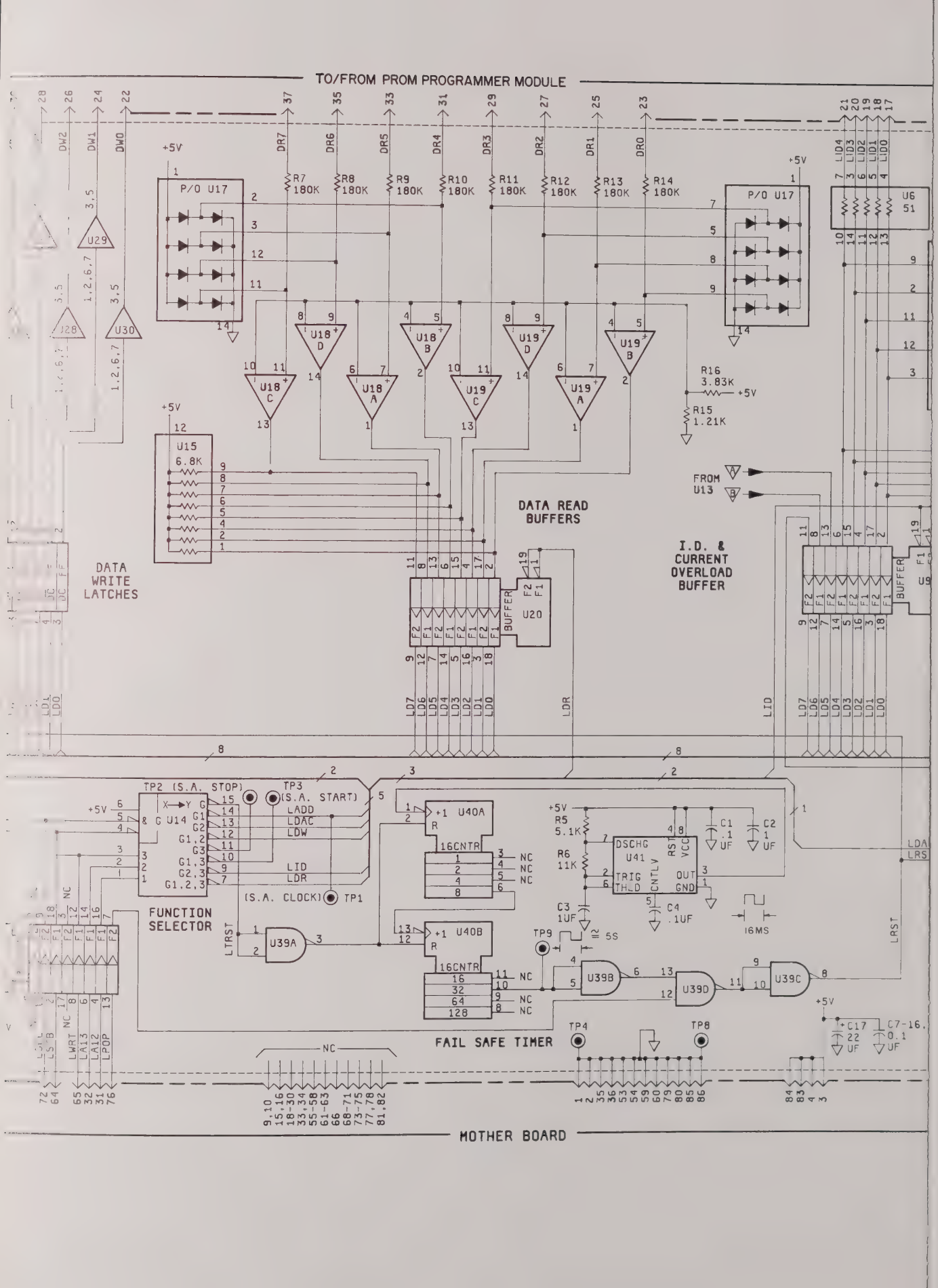
Mnemonic	Description
LSTB	Low Strobe -- when LSTB and LWRT are both low, the CPU is writing to a device over the CPU's Data Bus. If LSEL is also low, the PROM Programmer will recieve the information. If LSEL is high, the PROM Programmer will not pay attention to the information sent on the bus. If LSTB is low, and LWRT is high, and the PROM Programmer is selected (LSEL low), then the PROM Programmer will return information to the CPU over the CPU's Data Bus.
LTRST	Low Timer Reset -- Resets the failsafe timer when low.
LWRT	Low Write -- when low, indicates the CPU is writing to the addressed device.
VP1-2	Voltage, Programmable 1 and 2 -- Adjustable Regulators used for developing various voltages and waveforms used for programming PROMs. The adjustable inputs (VP1R and VP2R) can be connected to LP1 and LP2 or to voltage dividers located on the Programmer Modules.
VP1R, VP2R	Voltage, Programmable Regulated -- Inputs to VR3 and VR4 which program thier outputs to +1.2 volts above VP1R and VP2R respectively.
VP3	Voltage, Programmable 3 -- Output of voltage regulator VR2 used for developing various voltage levels used for programming PROMs. VP3 is under program control due to DAC U21.





A		B		C		D		E		F		G	
REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-2	C18	C-4	CR2	F-4	R12	C-5	R29	G-5	TP10	F-2	U17	D-5	U34	B-2
C2	B-1	C19	B-4	CR3	A-2	R13	C-5	R30	F-4	U1	A-7	U18	D-5	U35	C-2
C3	B-1	C20	C-4	CR4	B-2	R14	C-5	R31	B-2	U2	B-7	U19	E-5	U36	C-2
C4	B-1	C21	G-4	MP1	F-3	R15	E-5	R32	A-2	U3	C-6	U20	F-5	U37	C-2
C5	D-3	C22	G-5	MP2	C-3	R16	E-5	R33	A-2	U4	C-6	U21	G-5	U38	D-2
C6	G-6	C23	G-4	Q1	D-3	R17	D-3	R34	A-3	U5	D-7	U22	A-5	U39	D-2
C7	B-7	C24	G-5	R1	D-6	R18	B-4	R35	A-3	U6	D-6	U23	B-4	U40	D-2
C8	D-6	C25	E-6	R2	D-6	R19	B-4	R36	A-6	U7	E-6	U24	C-4	U41	B-2
C9	E-6	C26	F-4	R3	B-2	R20	D-4	TP1	D-7	U8	F-6	U25	C-4	VR1	A-3
C10	G-5	C27	E-4	R4	B-2	R21	D-4	TP2	E-7	U9	F-6	U26	D-4	VR2	C-4
C11	A-5	C28	E-1	R5	B-2	R22	D-3	TP3	E-7	U10	G-6	U27	D-4	VR3	F-4
C12	D-5	C29	F-1	R6	B-2	R23	A-4	TP4	E-6	U11	A-6	U28	D-4	VR4	F-2
C13	F-5	C30	E-6	R7	C-5	R24	A-4	TP5	G-6	U12	B-6	U29	E-4	VR5	D-2
C14	B-4	C31	A-3	R8	C-5	R25	D-3	TP6	B-4	U13	D-6	U30	E-4	VR6	B-3
C15	E-4	C32	B-3	R9	C-5	R26	G-4	TP7	E-4	U14	D-6	U31	F-4		
C16	C-3	C33	D-2	R10	C-5	R27	E-6	TP8	C-1	U15	E-5	U32	G-4		
C17	A-2	CR1	D-3	R11	C-5	R28	G-6	TP9	D-9	U16	A-5	U33	B-3		


64501-66502
J1
A15 A14 A13 A12 A11 A10 A9 A8
A7 A6 A5 A4 A3 A2 A1 A0
U11 51
U1 51
U16 A,B
LP2
1,2,6,7
TO U9
+5V
R1 150
R2 150
U12
U2
U4 6.8K
U3 6.8K
ADDRESS LATCHES
U13 LATCH
U5 LATCH
LADD
J36 BUFFER
F1 F2
LD15 LD14 LD13 LD12 LD11 LD10 LD9 LD8
LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0
BI-DIR BUFFER F(ALL) G1/G2
U35
U34
R3 1K
BOARD IDENTIFICATION
P1
CPU DATA BUS
U31 LATCH
U24
U25
DW6
DW5


TO/FROM PROM PROGRAMMER MODULE
DW2
DW1
DW0
DR7
DR6
DR5
DR4
DR3
DR2
DR1
DR0
+5V
P/O U17
R7 180K
R8 180K
R9 180K
R10 180K
R11 180K
R12 180K
R13 180K
R14 180K
U6 51
U29
U30
J28
U18 D
U18 B
U19 D
U19 B
U18 C
U18 A
U19 C
U19 A
R16 3.83K
R15 1.21K
U15 6.8K
DATA WRITE LATCHES
DATA READ BUFFERS
I.D. & CURRENT OVERLOAD BUFFER
FROM U13
U20
BUFFER
U9
LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0
LDR
LID
TP2 (S.A. STOP)
TP3 (S.A. START)
(S.A. CLOCK) TP1
FUNCTION SELECTOR
LADD
LDAC
LDW
LID
LDR
U40A
U40B
16CNTR
U39A
U39B
U39C
U39D
U41
DSCHG
TRIG
THLD
CNTLV
RST
VCC
OUT
GND
R5 5.1K
R6 11K
C1 .1 UF
C2 1 UF
C3 1UF
C4 .1UF
16MS
5S
LDA
LRS
LRST
LTRST
FAIL SAFE TIMER
TP4
TP8
TP9
C17 22 UF
C7-16, 0.1 UF
LWRT
LA13
LA12
LPOP
MOTHER BOARD

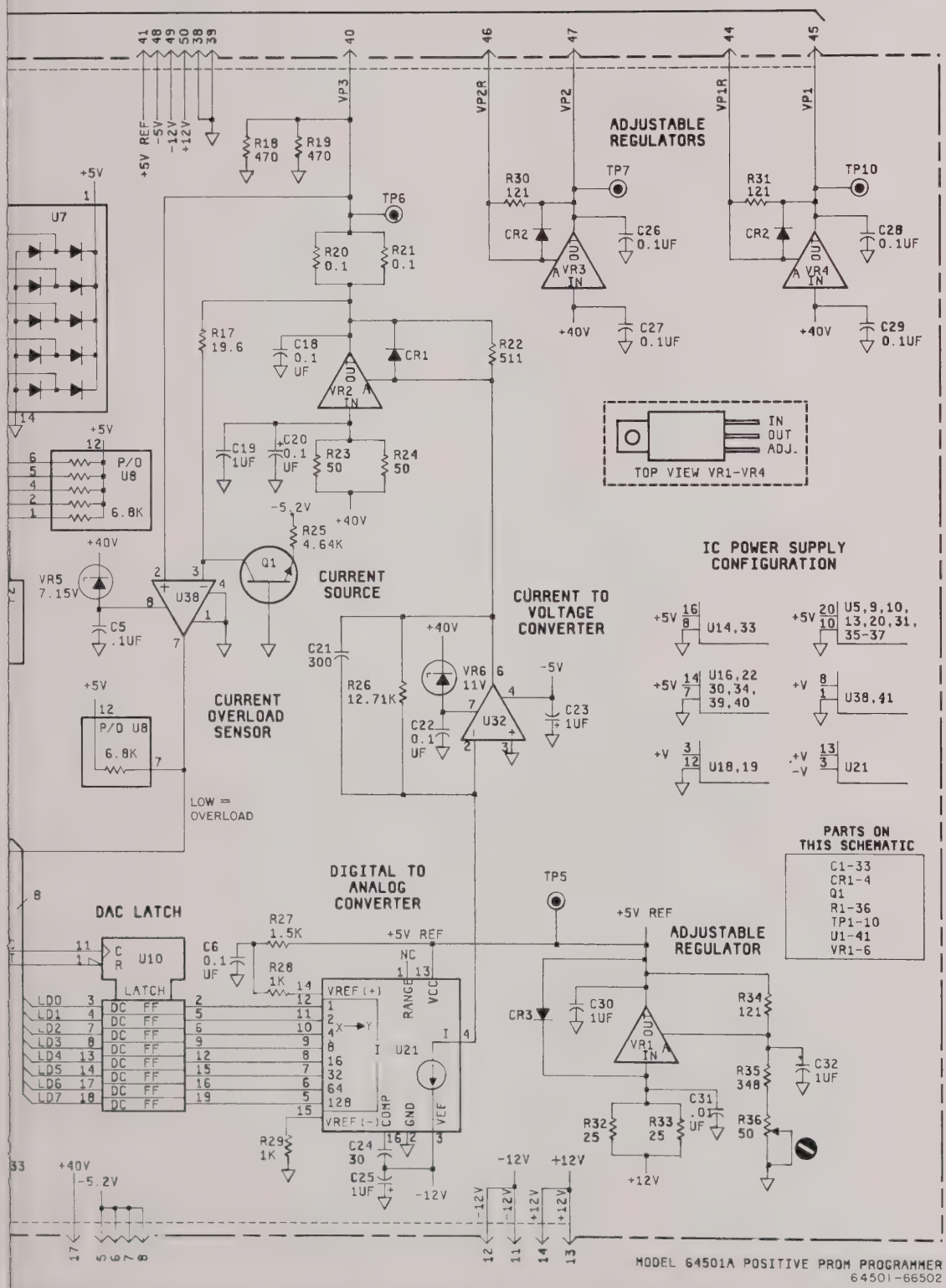


Figure 8-2.
PROM Programmer
PROM Prog 8-11

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March 1983 5952-6900

HP distributors are printed in italics.

64500-90910, OCTOBER 1982
Replaces: 64500-90908, May 1981

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PRINTED IN U.S.A.

MP MASTER
MA27218
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